



PCI-SIG ENGINEERING CHANGE NOTICE

TITLE:	PCI Express Base PCI Bus Power Management Spec Updates
DATE:	January 7, 2005
AFFECTED DOCUMENT:	PCI Express Base Specification 1.0a
SPONSOR:	Ken Stufflebeam : Microsoft Corporation

Part I

1. Summary of the Functional Changes

This ECR updates the PCI Express Base Specification to come into line with revision 1.2 of the PCI Bus Power Management Specification.

Section 5.1 and 5.3.1 and 7.6 – corrected revision reference to PCI BPMS

Section 5.3.1.4 – corrected text regarding the requirement for devices to preserve functional context when software transitioned from D3hot to D0

Section 5.3.1.4.1 – added note regarding No_Soft_Reset when software transitioned from D3hot to D0

Figure 7-16 – corrected fields to reflect PCI Express reserved and No_Soft_Reset bits

2. Benefits as a Result of the Changes

Current version of PCI Bus Power Management Specification is 1.2, not 1.1 as noted several places.

Text regarding No_Soft_Reset flag enables functions to maintain context when software transitioned from D3hot to D0 meaning they do not have to undergo an initialization sequence. This is a new feature from 1.1 to 1.2 and unless designers are current with the PCI BPMS, they are not aware of this feature.

Current Power Management Status/Control register does not show the new bits defined with revision 1.2. Since figure is included, it should be updated to reflect current configuration.

3. Assessment of the Impact

Minor but necessary updates

4. Analysis of the Hardware Implications

No required changes. No_Soft_Reset is a new feature defined to be backwards compatible with designs that are not aware of it. Implementation of this feature is appropriate for many designs. The ramifications of implementing this feature are discussed in PCI BPM 1.2.

5. Analysis of the Software Implications

No required changes. Software that is aware of the No_Soft_Reset bit may avoid re-initialization of functions resuming from the D3 state thus reducing resume time when returning functions from D3 to D0.

Part II

Detailed Description of the change

Change reference to current PCI BPMS in section 5.1. Overview:

PCI Express-PM is compatible with the PCI Bus Power Management Interface Specification, Revision 1.1-2 (PCI-PM), and the Advanced Configuration and Power Interface Specification, Revision 2.0 (ACPI). This chapter also defines PCI Express native power management extensions. These provide additional power management capabilities beyond the scope of the PCI Power Management Interface Specification.

Add revision reference to PCI BPMS in section 5.3.1 Device Power Management States (D-States) of a Function:

PCI Express supports all PCI-PM device power management states. All functions must support the D0 and D3 states (both D3_{hot} and D3_{cold}). The D1 and D2 states are optional. Refer to the *PCI Bus Power Management Interface Specification, Revision 1.2*, for further detail relating to the PCI-PM compatible features described in this specification. Note that where this specification defines detail that departs from the *PCI Bus Power Management Interface Specification*, this specification takes precedence for PCI Express components and Link hierarchies.

Correct reference to saving of functional context in D3hot state and explain the use of the no soft reset bit in PCI BPMS's PMCS register in section 5.3.1.4. D3 State:

D3 support is required, (both the D3_{cold} and the D3_{hot} states). Functions supporting PME generation from D3 must support it for both D3_{cold} and the D3_{hot} states.

~~Functional context does not need to be maintained by functions in the D3 state. Software is required to re-initialize the function following a D3 → D0 transition.~~

Functional context is required to be maintained by functions in the D3_{HOT} state if the No_Soft_Reset field in the Power Management Control/Status register is set to 1. In this case, software is not required to re-initialize the function after a transition from D3_{HOT} to D0 (the device will be in the D0_{initialized} state). If the No_Soft_Reset bit is set to 0, functional context is not required to be maintained by the function in the D3_{HOT} state. As a result, in this case software is required to fully re-initialize the function after a transition to D0 as the device will be in the D0_{uninitialized} state.

The device will be reset if the link state has transitioned to the L2/L3 Ready state regardless of the value of the No_Soft_Reset bit.



IMPLEMENTATION NOTE

Transitioning to L2/L3 Ready

As described in Section 5.2, transition to the L2/L3 Ready state is initiated by platform power management software in order to begin the process of removing main power and

clocks from the device. As a result, it is expected that a device will transition to D3 Cold shortly after its link transitions to L2/L3 Ready, making the No Soft Reset bit, which only applies to D3 Hot, irrelevant. While there is no guarantee of this correlation between L2/L3 Ready and D3 Cold, system software should ensure that the L2/L3 Ready state is entered only when the intent is to remove device main power. Devices, including those that are otherwise capable of maintaining functional context while in D3 Hot (i.e. set the No Soft Reset bit), are required to re-initialize internal state as described in Section 2.9.1 when exiting L2/L3 Ready due to the required DL Down status indication.

Add note regarding no soft reset bit in PCI BPMS's PMCSR to section 5.3.1.4.1. D3_{hot} State:

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Functions that are in D3_{hot} may be transitioned by software (writing to their PMCSR PowerState field) to the D0_{initialized} or the D0_{uninitialized} state. Note that the function is not required to generate an internal hardware reset during or immediately following its transition from D3_{hot} to D0_{uninitialized}. (see usage of the No_Soft_Reset bit in the PMCSR).

Spell out revision in reference to PCI BPMS in section 7.6 PCI Power Management Capability Structure:

This structure is required for all PCI Express devices. This capability is defined in the PCI Bus Power Management Interface Specification, ~~Rev~~ Revision 1.2. The functionality associated with this structure is the same for PCI Express as it is for conventional PCI, and only the added requirements associated with PCI Express are included here.

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Add "No_Soft_Reset" and "Reserved for PCI Express" bits in Figure 7-16: Power Mangement Status/Control Register:

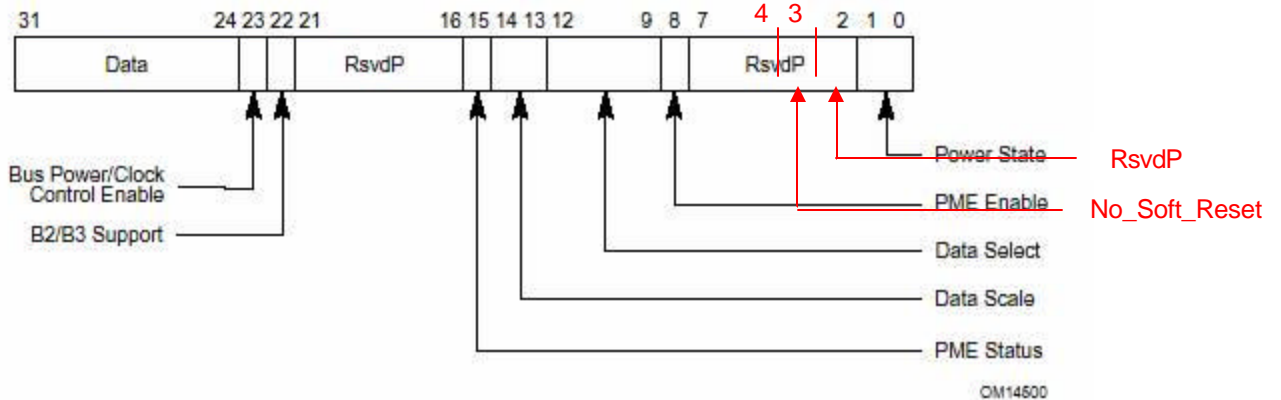


Figure 7-16: Power Management Status/Control Register

