

1. PCI Engineering Change Notice – Reset Limit Adjustment

TITLE:	Reset Limit Adjustment
DATE:	July 17, 2003
AFFECTED DOCUMENT(S):	PCI Express 1.0a
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1.1. Summary of the Functional Changes

Proposes to reduce the time limit from end of Fundamental Reset to the entry to LTSSM Detect state from 80ms to 20ms. Removes implementation note regarding PERST#. Other minor edits.

1.2. Benefits

Clarifies relationship between PERST# and fundamental reset. Resolves conflict between two timing parameters.

1.3. Assessment of the Impact

Reduces time limit. Not expected to impact most implementations.

1.4. Analysis of the Hardware Implications

Reduces time limit. Not expected to impact most implementations.

1.5 Analysis of the Software Implications

Clarifies fundamental reset.

1.6 Additional Description and Rationale

Fundamental Reset Clarification

Introduction

This ECR proposes to clarify the relationship between PERST# and fundamental reset and to fix an inconsistency between two reset related timing parameters.

Specification Document Changes

On p. 164:

The Port LTSSM (see Section 4.2.5) is initialized (see Section 6.6 for additional requirements) ~~(i.e., Detect is immediately entered).~~

On p. 289:

When PERST# is provided to a component or add-in card, this signal must be used by the component or add-in card ~~as to cause a~~ Fundamental Reset.

On p. 290:

A component must enter the ~~LTSSM Detect initial active Link Training~~ state within ~~2080~~ ms of the end of Fundamental Reset (Link Training is described in Section 4.2.4)

Delete the implementation note in 6.6, p.292:

~~IMPLEMENTATION NOTE~~

~~Use of PERST# The deassertion of PERST# may not be sufficient in all implementations to say that fundamental reset is exited. Such implementations may require other additional conditions to be met; for example, the I/O PLL locking, before exiting fundamental reset.~~