



PCI-SIG ENGINEERING CHANGE NOTICE

TITLE:	Bridge Related Updates
DATE:	August 21, 2003
AFFECTED DOCUMENT:	PCI Express Base Specification, Rev 1.0a
SPONSOR:	Carl Jackson; Hewlett-Packard Company Sridhar Muthrasanallur; Intel Corporation

Part I

1. Summary of the Functional Changes

Update the PCI Express Base Specification, Revision 1.0a to comprehend functionality introduced in the PCI Express to PCI/PCI-X Bridge Specification, Revision 1.0. Specifically:

1. Reference the PCI Express Vendor-Defined Message / PCI-X Device ID Message interoperability rules contained in the PCI Express to PCI/PCI-X Bridge spec
2. Show the Bridge Configuration Retry Enable bit that was added to the Device Control Register of the PCI Express Capability Structure

2. Benefits as a Result of the Changes

Make designers aware of the additional requirements placed on Vendor-Defined Message Requests by the PCI Express to PCI/PCI-X Bridge spec when interoperability with PCI-X Device ID Messages is desired. Also update the PCI Express Base spec to show the usage of bit 15 in the Device Control Register of the PCI Express Capability Structure by PCI Express to PCI/PCI-X Bridges.

3. Assessment of the Impact

No impact to existing systems. Changes apply to new, optional functionality for all PCI Express devices or to functionality only applying to PCI Express to PCI/PCI-X Bridges as defined in the PCI Express to PCI/PCI-X Bridge spec

4. Analysis of the Hardware Implications

New PCI Express hardware can choose to implement Vendor-Defined Messages that are interoperable with PCI-X 2.0 Device ID Messages. Impact to PCI Express to PCI/PCI-X Bridges is already comprehended in the PCI Express to PCI/PCI-X Bridge spec.

5. Analysis of the Software Implications

No impact to existing software. New software may be required to enable new message functionality. Impact to PCI Express to PCI/PCI-X Bridge-aware software is already comprehended in the PCI Express to PCI/PCI-X Bridge spec.

Part II

Detailed Description of the change

a) Vendor_Defined Message

The following two changes update the PCI Express Base spec to reference the additional requirements noted in the PCI Express to PCI/PCI-X Bridge spec for Vendor_Defined Messages that are intended to be interoperable with PCI-X Device ID Messages.

Section 2.2.6.2, p.55 – Modify bullet beginning on line 16 as follows:

- For Requests which do not require a Completion (Posted Requests), the value in the Tag[7:0] field is undefined and may contain any value. (See Section 2.2.8.6. for exceptions to this rule for certain Vendor Defined Messages.)

Section 2.2.8.6, p.71 – Add the following paragraph to the end of this section:

The PCI Express to PCI/PCI-X Bridge Specification, Rev. 1.0 defines additional requirements for Vendor Defined Messages that are designed to be interoperable with PCI-X Device ID Messages. This includes restrictions on the contents of the Tag[7:0] field and the Length[9:0] field as well as specific use of Bytes 12 through 15 of the message header. Vendor Defined Messages intended for use solely within a PCI Express environment (i.e., not intended to address targets behind a PCI Express to PCI/PCI-X Bridge) are not subject to the additional rules. See PCI Express to PCI/PCI-X Bridge 1.0 for details.

b) Bridge Configuration Retry Enable

The following two changes update the PCI Express Base spec to show the usage by PCI Express to PCI/PCI-X Bridges of a previously reserved bit (bit 15) in the Device Control Register of the PCI Express Capability Structure. Software uses this bit to enable PCI Express to PCI/PCI-X Bridges to return Completions with Configuration Request Retry Status. Details are contained in PCI Express to PCI/PCI-X Bridge 1.0.

Section 7.8.4, p.341 – Modify Figure 7-14 as follows:

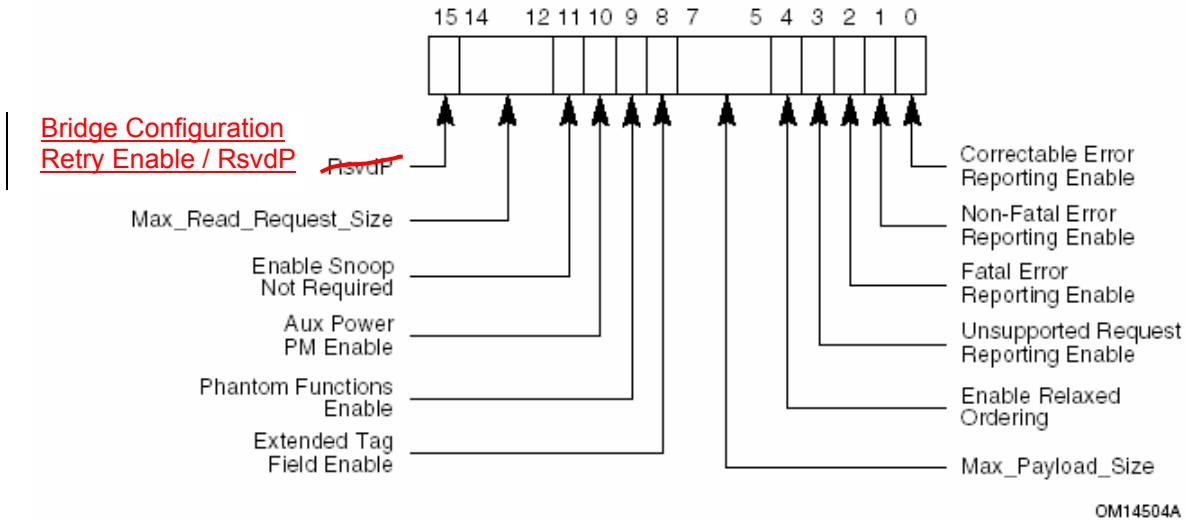


Figure 7-14: Device Control Register

Section 7.8.4, p.344 – Add to the end of Table 7-12 as follows:

Table 7-12: Device Control Register

Bit Location	Register Description	Attributes
15	<p><u>PCI Express to PCI/PCI-X Bridges:</u></p> <p>Bridge Configuration Retry Enable – When set, this bit enables PCI Express to PCI/PCI-X bridges to return Configuration Request Retry Status (CRS) in response to Configuration Requests that target devices below the bridge. Refer to the <u>PCI Express to PCI/PCI-X Bridge Specification, Rev. 1.0</u> for further details.</p> <p>Default value of this field is 0.</p> <p><u>All others:</u></p> <p>Reserved – must hardwire the field to 0b.</p>	<p><u>PCI Express to PCI/PCI-X Bridges:</u></p> <p><u>RW</u></p> <p><u>All others:</u></p> <p><u>RsvdP</u></p>

<End of ECN>