



## PCI-SIG ENGINEERING CHANGE NOTICE

|                           |  |
|---------------------------|--|
| <b>TITLE:</b>             | Platform Ref Clock PM Capability             |
| <b>DATE:</b>              | 12 Jan 2004                                  |
| <b>AFFECTED DOCUMENT:</b> | PCI Express Base Specification Revision 1.0a |
| <b>SPONSOR:</b>           | David Harriman, Intel Corporation            |

### **Part I**

#### **1. Summary of the Functional Changes**

Proposes to provide provision for an optional platform clock power management capability reporting mechanism for PCI Express based devices, and repairs related issue with Table 5-1. A configuration bit is defined to report whether a device supports power managing the reference clock. Current implementations do not include this bit and so will appear as not supporting this feature (indicating that the platform must provide an unqualified (free-running) reference clock to the device per the PCI Express specification). This ensures backwards compatibility.

In order to support this new capability, a device must implement the L1 & L2/3 Ready link states in a manner that allows the reference clock to be put in the parked clock state. The device de-asserts its clock request output after it has put all links in the L1 (L2/3 Ready) link state and asserts its clock request as the first step of returning any of its links to the L0 link state.

#### **2. Benefits as a Result of the Changes**

Platform clock power management is important to mobile client PC and handheld client applications, particularly when at least one reference clock is required for each PCI Express device.

#### **3. Assessment of the Impact**

No impact to existing implementations. Provides for future benefit.

#### **4. Analysis of the Hardware Implications**

Future hardware intending to support this behavior will have additional design to account for PLL tolerance to shutting down the reference clock, additional delays (in the order of 50 ns) and comprehending CLKREQ# protocol.

#### **5. Analysis of the Software Implications**

No impact to existing software. However, future software development should comprehend this new capability.

## Part II

### Detailed Description of the change

In table 5.1:

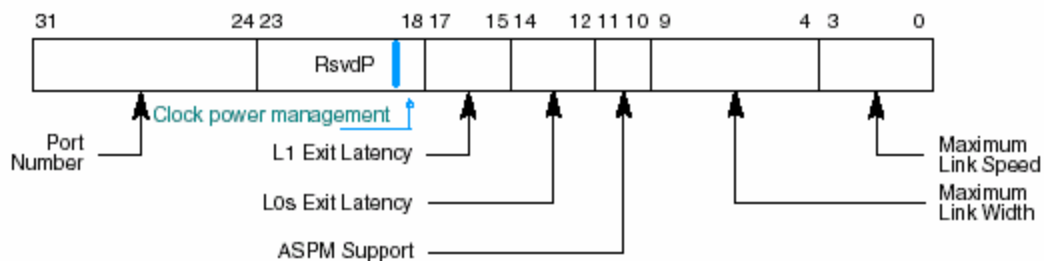
**Table 5-1: Summary of PCI Express Link Power Management States**

|             | L state description             | SW directed PM   | Used by ASPM               | Platform reference clock                   | Platform main power | Component internal PLL | Platform Vaux   |
|-------------|---------------------------------|------------------|----------------------------|--|---------------------|------------------------|-----------------|
| L0          | Fully active link               | Yes (D0)         | Yes (D0)                   | On   | On                  | On                     | On/Off          |
| L0s         | Standby state                   | No               | Yes <sup>1</sup> (D0)      | On   | On                  | On                     | On/Off          |
| L1          | Low power standby               | Yes (D1-D3hot)   | Yes <sup>2</sup> (opt. D0) | <del>On</del><br><u>On/Off<sup>7</sup></u> | On                  | On/Off <sup>3</sup>    | On/Off          |
| L2/L3 Ready | Staging point for power removal | Yes <sup>4</sup> | No                         | <del>On</del><br><u>On/Off<sup>7</sup></u> | On                  | On/Off                 | On/Off          |
| L2          | Low power sleep state           | Yes <sup>5</sup> | No                         | Off  | Off                 | Off                    | On <sup>6</sup> |
| L3          | Off                             | n/a              | n/a                        | Off  | Off                 | Off                    | Off             |

Notes:

7. Low power mobile or handheld platforms may aggressively reduce power by clock gating the reference clock(s). As a result, components targeting these platforms should be tolerant of the additional delays required to re-energize the reference clock during the low power state exit.

In Figure 7-16, label bit 18 (indicated) of the link capabilities register:



CM14506A

**Figure 7-16: Link Capabilities Register**

In Table 7-14, add description for bit 18:

Table 7-14: Link Capabilities Register

| Bit Location | Register Description  | Attributes |
|--------------|---|------------|
| 17:15        | ...   |            |
| <u>18</u>    | <p><b>Clock Power Management-</b> A value of 1b in this bit indicates that the component tolerates the removal of any reference clock(s) when the link is in the L1 and L2/3 Ready link states. A value of 0b indicates the component does not have this capability and that reference clock(s) must not be removed in these link states.</p> <p>This capability is applicable only in form factors that support "clock request" (CLKREQ#) capability</p> <p>For a multi-function device, each function indicates its capability independently. Power Management configuration software must only permit reference clock removal if all functions of the multi-function device indicate a 1b in this bit.</p> | <b>RO</b>  |
| 31:24        | ...   |            |

In Figure 7-17, label bit 8 (indicated) of the link control register:

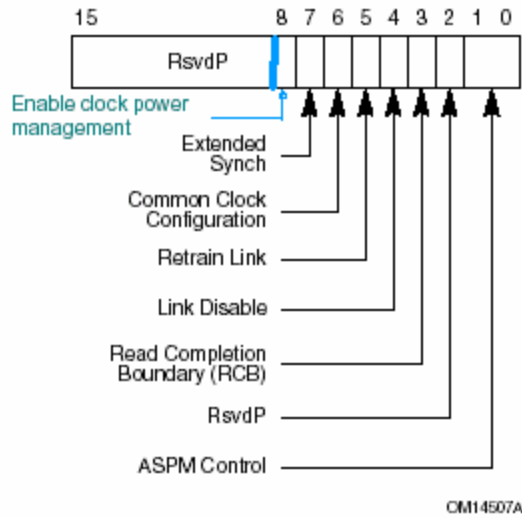


Figure 7-17: Link Control Register

In Table 7-15, add description for bit 8:

Table 7-15: Link Control Register

| Bit Location | Register Description  | Attributes       |
|--------------|---|------------------|
| 7            | ...   |                  |
| <u>8</u>     | <p><b>Enable Clock Power Management</b> – Applicable only for form factors that support a “Clock Request” (CLKREQ#) mechanism, this enable functions as follows:</p> <p>0b – Clock power management is disabled and device must hold CLKREQ# signal low</p> <p>1b - When this bit is set to 1 the device is permitted to use CLKREQ# signal to power manage link clock according to protocol defined in appropriate form factor specification.</p> <p>Default value for this field is 0b.</p> <p>Components that do not support Clock Power Management (as indicated by a 0b value in the Clock Power Management bit of the Link Capabilities Register) must hardwire this bit to 0b.</p> | <b><u>RW</u></b> |