



PCI-SIG ENGINEERING CHANGE NOTICE

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|---------------------------|--|
| TITLE: | Training Error Removal |
| DATE: | 4 Aug 2003 (reformatted 12 Dec 2003) |
| AFFECTED DOCUMENT: | PCI Express Base Specification Revision 1.0a |
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Part I

1. Summary of the Functional Changes

Removes Training Error from the specification. The following are affected: Definition (Ch4), references (Ch6), configuration bits (Ch7).

2. Benefits as a Result of the Changes

Training Error has not been well defined, and as a consequence, has limited usefulness. Since it is a fatal error, false triggering is highly undesirable, and so by removing the error we can eliminate this risk.

3. Assessment of the Impact

Removes currently defined error. Existing hardware potentially subject to false triggering (above).

4. Analysis of the Hardware Implications

Removes currently defined error.

5. Analysis of the Software Implications

Existing software potentially affected if it acts on reporting of Training Error. Changes are implemented to minimize likelihood of interoperability problems.

Part II

Detailed Description of the change

In 2.2.8.3. Error Signaling Messages:

Error Signaling Messages are used to signal errors that occur on specific transactions and errors that are not necessarily associated with a particular transaction ~~(e.g., Link training fails)~~. These Messages are initiated by the agent that detected the error.

In 4.2.4. Link Initialization and Training:

...

~~Receivers may optionally check for violations of the Link Initialization and Training Protocols. If such checking is implemented, any violation is a Training Error. A Training Error is a reported error associated with the Port (see Section 6.2). A Training Error is considered fatal to the Link.~~

In 6.2.6. Error Listing and Rules, Table 6-2:

Table 6-2: Physical Layer Error List

| Error Name | Default Severity | Detecting Agent Action |
|---------------------------|----------------------------------|--|
| Receiver Error | Correctable | <i>Receiver (if checking): Send ERR_COR to Root Complex.</i> |
| Training Error | Uncorrectable (Fatal) | If checking, send ERR_FATAL to Root Complex. [footnote: Only the component closer to the Root Complex is typically capable of sending the error Message.] |

In 7.8.8. Link Status Register :

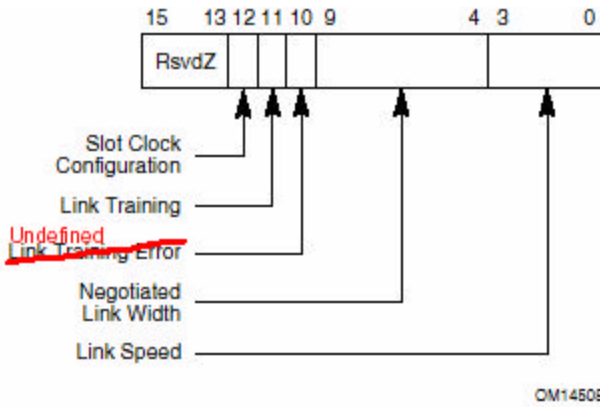


Figure 7-18: Link Status Register

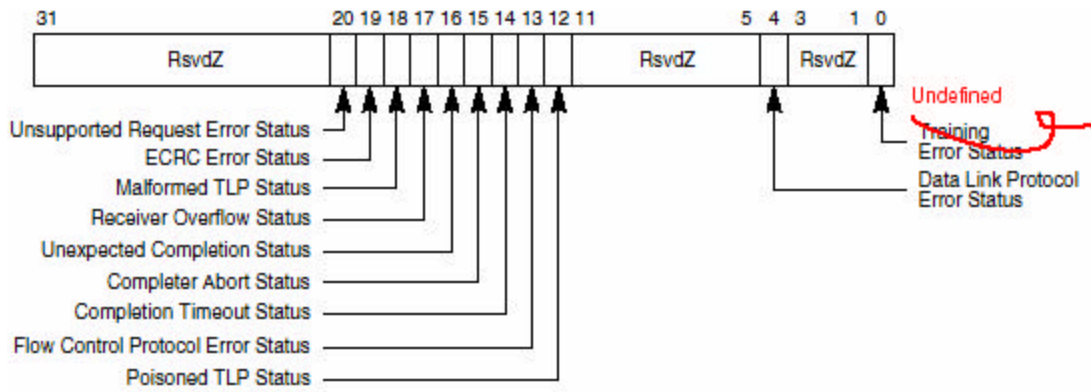
Table 7-16: Link Status Register

| Bit Location | Register Description | Attributes |
|--------------|--|------------|
| ... | | |
| 10 | <p>Training Error – This read-only bit indicates that a Link training error occurred.</p> <p>This field is not applicable and reserved for Endpoint devices and Upstream Ports of Switches.</p> <p>This bit is cleared by hardware upon successful training of the Link to the L0 Link state.</p> <p>Undefined – The value read from this bit is undefined. In previous versions of this specification, this bit was used to indicate a Link Training Error. System software must ignore the value read from this bit. System software is permitted to write any value to this bit.</p> | RO |
| 11 | <p>Link Training – This read-only bit indicates that Link training is in progress (the Physical Layer LTSSM is in the Configuration or Recovery state,) or that 1b was written to the Retrain Link bit but Link training has not yet begun. Hardware clears this bit when the LTSSM exits the Configuration/Recovery state once Link training is complete.</p> <p>This field is not applicable and reserved for Endpoint devices and Upstream Ports of Switches, and must be hardwired to 0b.</p> | RO |
| ... | | |

In 7.10.2. Uncorrectable Error Status Register:

...

In Figure, label bit 0 (indicated) as RsvdZ-



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Figure 7-28: Uncorrectable Error Status Register

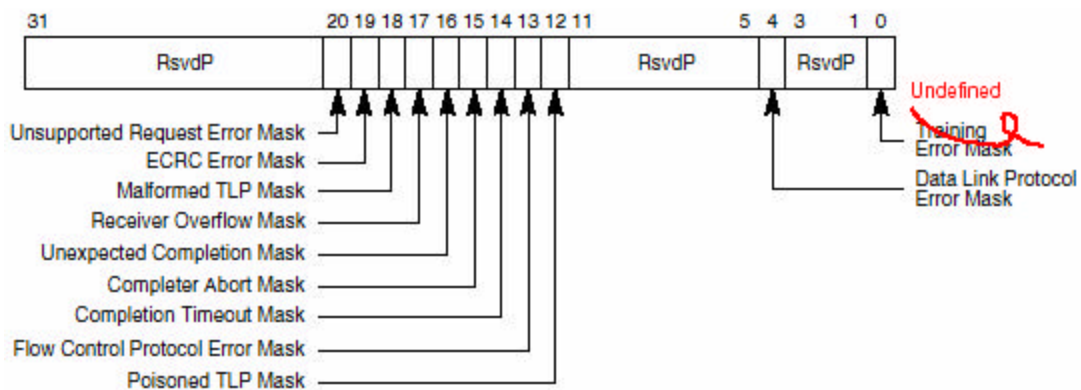
Table 7-24: Uncorrectable Error Status Register

| Bit Location | Register Description | Attributes | Default Value |
|--------------|---|-------------------------------|----------------|
| 0 | Training Error Status (Optional) Undefined - The value read from this bit is undefined. In previous versions of this specification, this bit was used to indicate a Link Training Error. System software must ignore the value read from this bit. System software is permitted to write any value to this bit. | RW1CS Undefined | 0 Undefined |
| ... | | | |

In 7.10.3 Uncorrectable Error Mask Register:

...

In Figure, label bit 0 (indicated) as RsvdP-



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Figure 7-29: Uncorrectable Error Mask Register

Table 7-25: Uncorrectable Error Mask Register

| Bit Location | Register Description | Attributes | Default Value |
|--------------|--|------------------|----------------|
| 0 | Training Error Mask (Optional) Undefined - The value read from this bit is undefined. In previous versions of this specification, this bit was used to mask a Link Training Error. System software must ignore the value read from this bit. System software must only write a value of 1b to this bit. | RWS Undefined | 0 Undefined |
| ... | | | |

In 7.10.4, Uncorrectable Error Severity Register:

In Figure, label bit 0 (indicated) as RsvdP-

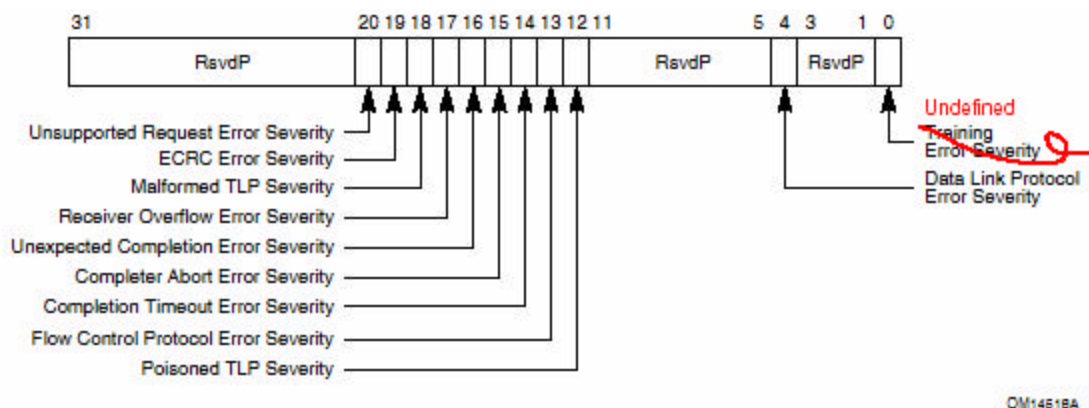


Figure 7-30: Uncorrectable Error Severity Register

Table 7-26: Uncorrectable Error Severity Register

| Bit Location | Register Description | Attributes | Default Value |
|--------------|---|------------------|----------------|
| 0 | Training Error Severity (Optional) Undefined - The value read from this bit is undefined. In previous versions of this specification, this bit was used to set the severity of a Link Training Error. System software must ignore the value read from this bit. System software is permitted to write any value to this bit. | RWS Undefined | 1 Undefined |
| ... | | | |