



PCI Express (Rev1.1) Test Methodology for PLL Loop Bandwidth Response in Add-in cards.

Testing Guide for:

**SyntheSys Research, Inc.'s PLL Analyzer Series BERTScope PLA
CRJ 125A-PCIE and PLL-PCIE**

April 2008

Revision 1.0

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Questions regarding this document or membership in the PCI-SIG may be forwarded to:

PCI-SIG 3855 SW 153 Drive Beaverton, OR, 97006

Phone: 503-619-0569 Fax: 503-644-6708

E-mail Administration@pcisig.com

<http://www.pcisig.com>

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Revision History

Revision	Date	Changes
1.0	26 Apr 08	Initial Release



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1 PLL Loop Response Test Methodology

1.1 Overview

The PLL Loop Response test measures the bandwidth and peaking of the PLL used in Add-in cards for generating the Tx clock from the distributed 100 MHz REF_CLK signal. The loop response is determined by substituting a test clock for the locally generated REF_CLK which contains a calibrated level of sinusoidal jitter. The PLL analyzer measures the transferred jitter by applying the transmitted compliance pattern output from the Add-in card under test into a reference PLL. The phase deviation is digitized and analyzed within the instrument to determine its spectral components. The frequency of the modulating sinusoidal jitter is incrementally swept, with measurement data taken at each frequency step. The instrument computes the PLL magnitude and phase, along with jitter transfer function automatically.

In addition to measuring the loop response, the PLL analyzer contains the synthesizer used to generate the jitter modulated REF_CLK. The jitter appears as true phase modulation in the REF_CLK output, maintaining a 50% duty factor at all times. This allows the PLL analyzer to be used with all types of clock generation PLLs, including those which incorporate dual edge phase detectors.

Incorporating the synthesizer within the instrument facilitates internal self calibration, eliminating the need for the user to manually normalize the test setup calibration. Once the cabling to the Compliance Base Board is connected, the user can begin testing immediately.

An external PC is used to host system control and report generation software. This program plots the PLL Loop Response, compares the measured bandwidth and peaking against the specification limits, and can generate a test report in hard copy or HTML file format.

1.2 Test Equipment Required

The following equipment is required for PLL Loop Response testing to revision 1.1 requirements:

- PLL Analyzer model CRJ 125A-PCIE or PLL-PCIE.
- PLL Analysis control software – supplied with PLL Analyzer.
- Compliance Base Board V 1.1, jumpers configured to source the REF_CLK from external input. A version 2.0 CBB can also be used for testing at 2.5 GT/s rate. The V2.0 CBB requires substituting SMA to SMP interconnecting cables and type SMP terminators described below.

- SMA-M 50 Ω terminators for unused lanes. See note below.
- SMA-M to SMA-M interconnect cables for Tx data out. Low loss, \approx 40 cm length. 2 required. Astrolab Minibend-16, p/n: 32081-2-29094C-16 or equivalent.
- SMA-M to SMA-M interconnect cables for REF_CLK in. \approx 0.5 m length. 2 required. Loss characteristics are not critical as frequency content is \approx 100 MHz.
- Host PC to operate application software. Windows 2000 or XP operating system. One free USB1.1 or 2.0 port. While not required to perform a PLL Loop Response test, a printer (either local or networked to the host PC) is required if the user desires hard copy output of the test reports. Results can be stored as HTML files for printing at a later time.
- USB cable, type A to Type B. Supplied with PLA Analyzer.
- ATX type PC Power supply, with outputs as required to power Add-in card to be tested through the CBB. A higher quality, low noise supply may be required for some Add-in cards.
- The use of ESD dissipating mats for the work surface and wrist straps for the operator are good practice and suggested to avoid damage to the Add-in card under test and other test equipment.

Note: As allowed in the PCI Express standard, some Add-In cards require termination of unused lanes in order to initiate generation of the compliance test pattern. The CBB may be configured with various combinations of connectors installed to access the Tx lanes. Lanes without access connectors will be properly terminated. PLL Loop response testing is performed by measuring the Tx output on lane 0 only. If the Add-in card under test requires termination of unused Tx lanes to initiate compliance pattern generation, the user will need to terminate the required lanes which have access connectors on the CBB.

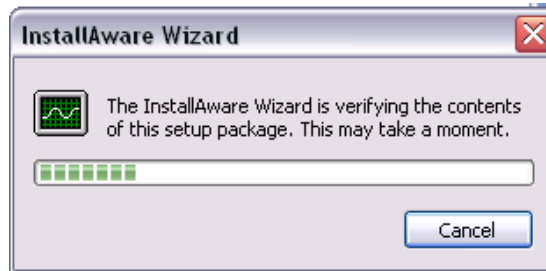
2 Test Preparation

2.1 Control Software Installation

Install the control software on the host PC before connecting the PLA Analyzer. The software only needs to be installed once on the host PC. It is installed from the CD-ROM supplied with the PLL Analyzer.

Turn on the power on the host PC and wait for the operating system to fully boot. Install the CD-ROM into the drive. The installer should autostart. Select CR_PCIE_PLL-Tester from the install menu choices. If the CD-ROM does not autostart, explore the CD-ROM root directory using My Computer or Explorer, locate the Setup_CR_PCIE_PLL.EXE file and double click to start installation.

The InstallAware Wizard with a progress indicator will appear.

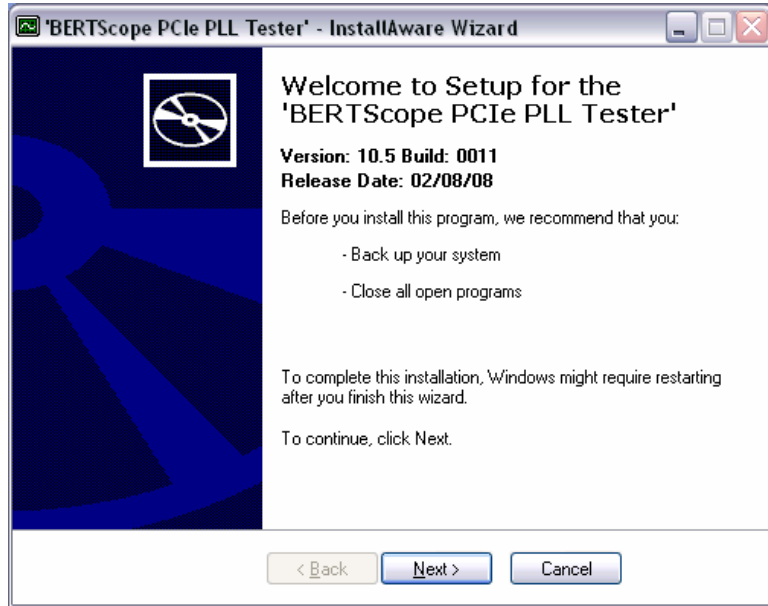


The screen showing the system requirements will then appear:



If the required add-ins are not installed, they can be downloaded for no charge from the Microsoft web site: www.microsoft.com.

When the following screen appears:

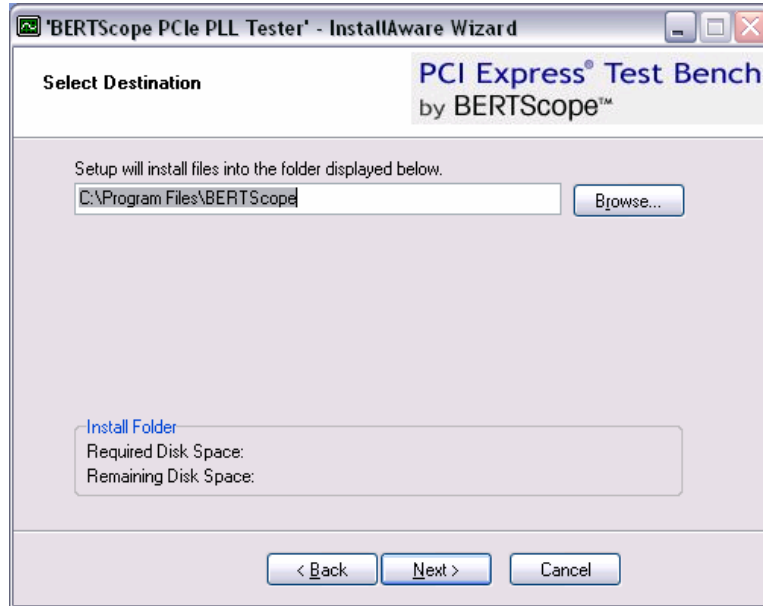


Click Next to continue.

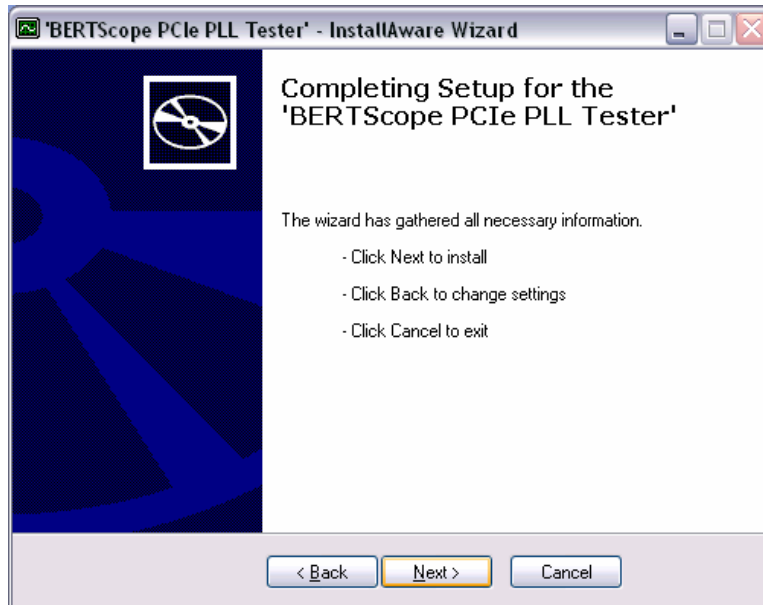
Select Typical Setup on the next screen, then click Next.



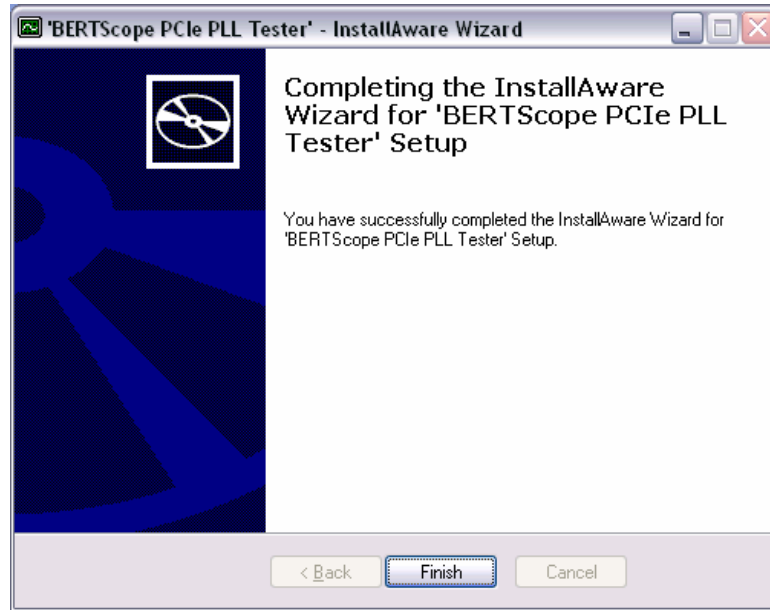
Select the default path on the next screen. Click Next



On the following screen, click Next to install.



A window with a progress bar will appear, showing the installation status. At the completion, the following window will appear:



Click Finish.

2.2 Installing the USB driver

The software installer has installed the control software and loaded, but did not install the USB driver for the PLL Analyzer. The user will be prompted to install the driver the first time the PLL Analyzer is connected to the host computer. The driver only needs to be installed once.

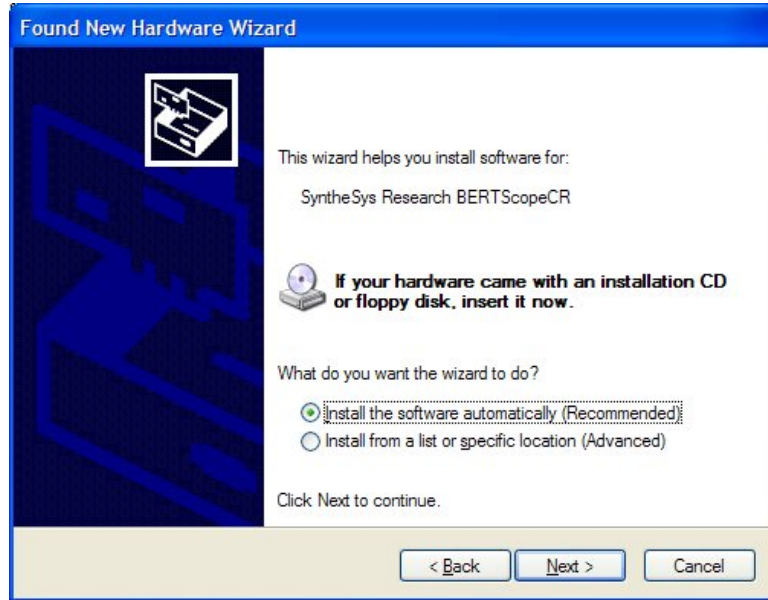
- Be sure the control software has been loaded from the CD-ROM as described in step 2.1 above.
- Power up the host PC and wait for the operating system to fully boot, if not already done. Do not start the PLL Analyzer application at this time.
- Connect the power cable of the PLL Analyzer to a live power outlet and push the power button.
- Using the supplied USB cable, connect the end with the type B connector to the receptacle labeled USB IN on the rear panel of the instrument.



- Connect the other end with the type A connector to an open USB port on the host PC.
- The “Found New Hardware” wizard notice will appear in the lower right side of the Windows Desktop screen. After the operating system detects the type of device, the installation wizard will start.
- The opening window will appear:



- Select the No, not this time radio button and then click Next. The Wizard identifies the device as a “Synthesys Research BERTScope CR”.



- Use the default Install the software automatically (Recommended) radio button option, then click Next.
- If the Hardware Installation dialog box stating that the driver has not been tested for “Windows XP compatibility” message pops up, press the Continue Anyway button.



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- After the Completion dialog windows appears, click Finish to complete installation.



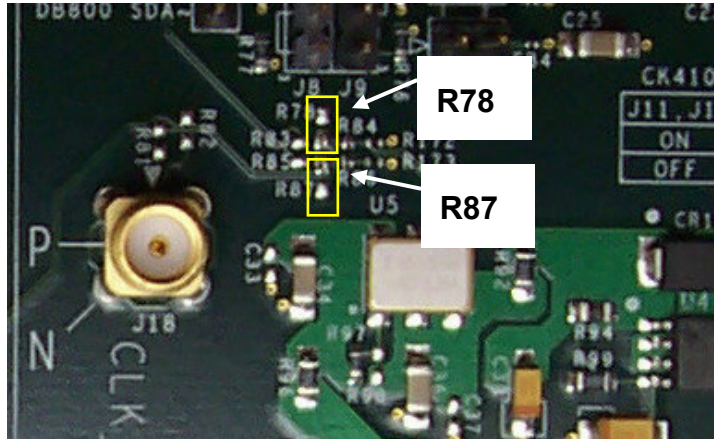
The instrument is now ready to operate.

2.3 Completing the PLL Analyzer test set-up

2.3.1 Configuring the Compliance Base Board (CBB)

The Compliance Base Board (CBB) jumpers must be configured to source the distributed REF_CLK from the input connectors. The CBB fixtures supplied from SyntheSys Research in the PCIE TEST KIT are already properly configured, and can be used immediately for PLL Loop Response testing.

The default configuration of the board as supplied by the PCI-SIG is with the REF_CLK signal supplied from an on-board clock generator. The configuration change to “REF CLK INJ” is performed by relocating jumpers on the CBB. The jumpers are surface mount devices (0 Ω resistors), and require a soldering iron to reposition. The jumpers are located near J18 the CLK_NOISE connector. The proper jumper locations are R78 and R87, are shown on the next page.



2.3.2 Hardware test set-up

Prior to configuring the test set-up, prepare the area for testing. It is suggested that an ESD dissipating mat be applied to the work surface. A grounding connection is located on the PLL Analyzer instrument.

Configure the instrument and cabling as described below:

1. Connect the supplied USB cable between the USB port on the host PC and the USB IN connector on the rear panel of the PLL Analyzer.



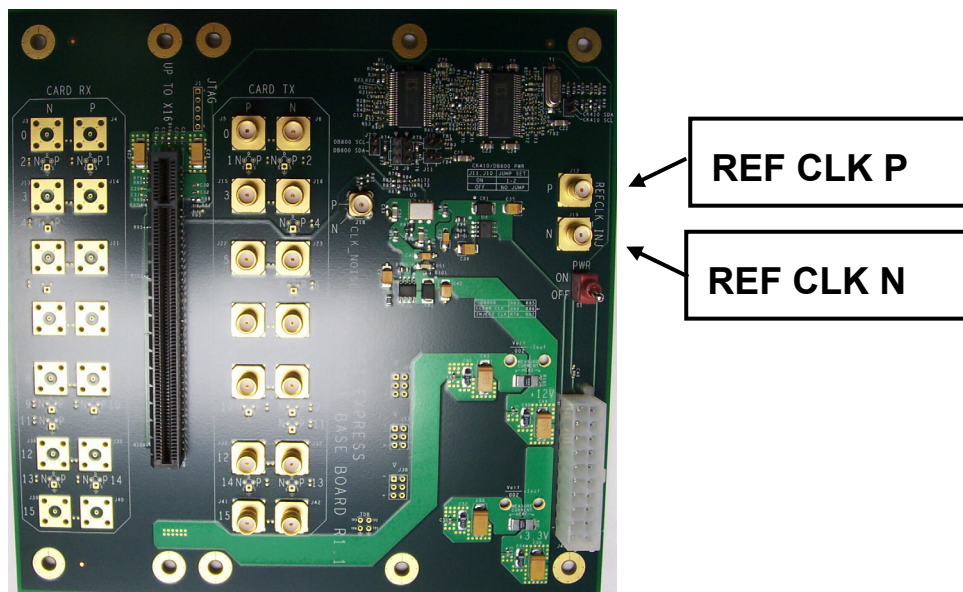
2. Connect the ATX PC Power Supply to the power connector on the Compliance Base Board (CBB)
3. Connect the longer SMA cables between the PCIe CLK+ output on the PLL Analyzer to the REF CLK P input connector on the CBB. Using the second cable, connect the PCIe CLK- output to the REF CLK- input of the CBB. Be sure to observe the proper polarity.

The PCIe CLK output connectors are located on the rear of the model CRJ 125A-PCIE instrument:



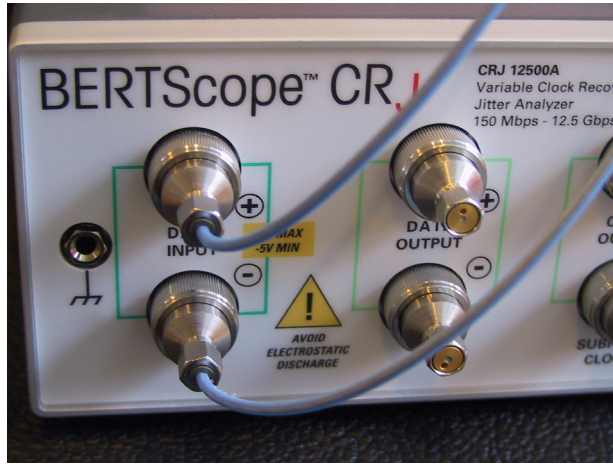
The PCIe CLK + and PCIe CLK- connectors are located on the front panel of the model PLL-PCIE analyzer.

The REF_CLK input connector locations on the CBB are shown below.

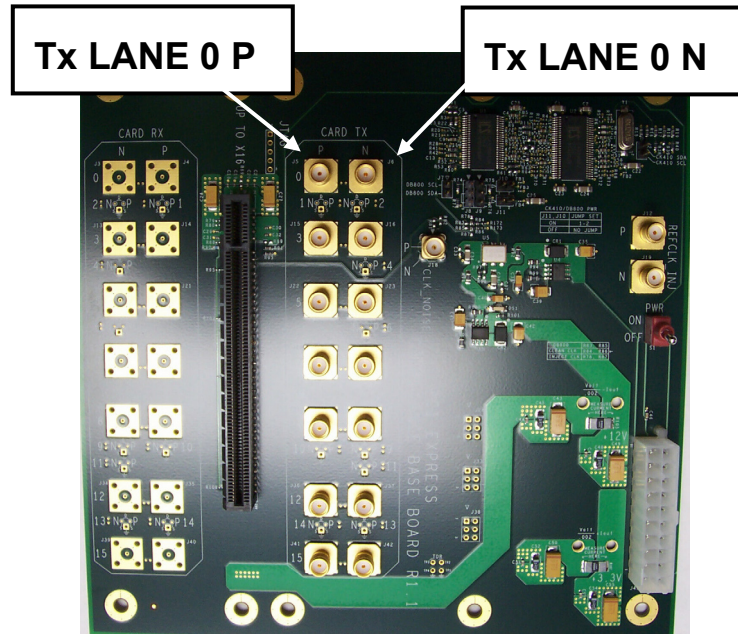


- Using the short, low loss SMA-M to SMA-M connectors, connect Tx LANE 0 P on the CBB to DATA INPUT + on the PLL Analyzer. Connect Tx LANE 0 N on the CBB to DATA INPUT - on the PLL Analyzer. The Data Input connectors are located on the front panel of the instrument.

NOTE: If a model CRJ 125A-PCIE analyzer is being used, the



Tx Lane 0 output connector location shown below.



5. If required by the Add-in card to initiate compliance output pattern, terminated unused Tx lanes with 50 Ω terminators.
6. For protection of the Add-in card under test, it is suggested that a ESD dissipating wrist strap be used by the operator. A grounding connector is located on the front panel of the PLL Analyzer.

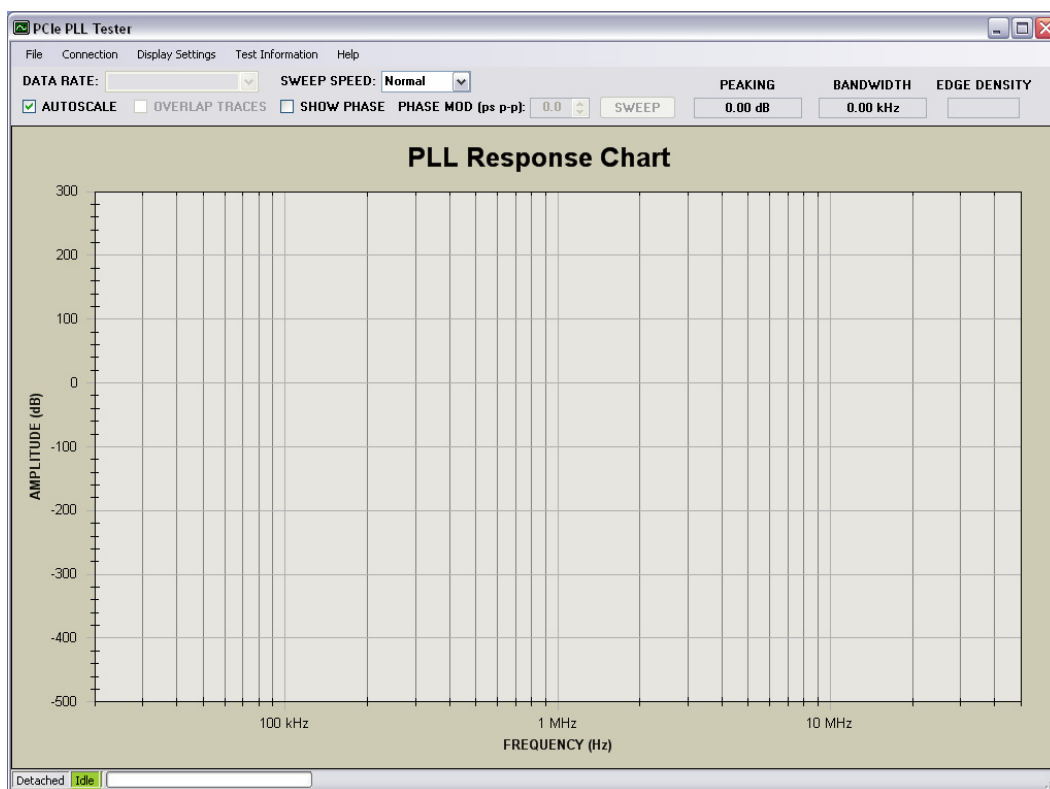
3 Testing PLL Loop Response

With the cable configuration completed, the system is ready to perform PLL Loop Response measurements. No user calibration or normalization steps are required.

Initiate the testing by powering up the host PC and the PLL Analyzer. Start the Control software application by clicking:

START – PROGRAMS – BERTScope – BERTScope PCIe PLL Tester

The application will open with the single window used for control and display:



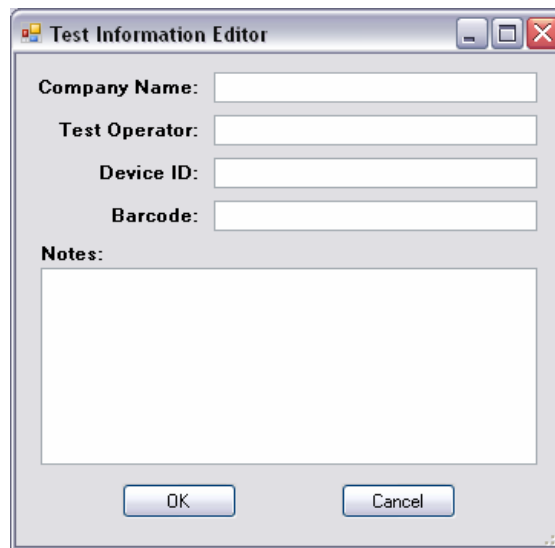
In the DATA RATE pull down menu, select 2.5 GT/s.

The phase modulation defaults to 43.4 ps, the maximum allowed by the compliance spec. This setting should be used for a normal compliance test. Other modulation levels can be entered to characterize sensitivity to modulation level, and observe test margin to this parameter.

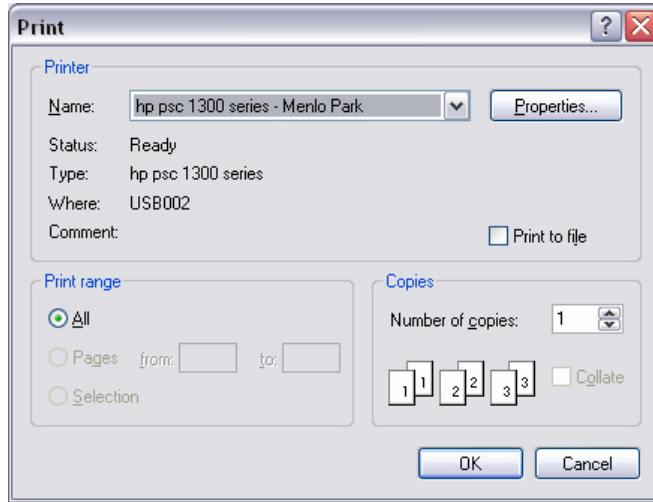
Perform the test using the following procedure.

1. Install the Add-in card to be tested into the socket on the CBB. Connect any required auxiliary power connectors to the ATX PC Power supply.
2. Turn on the power supply.

3. Turn on the device power using the PWR switch on the CBB.
 Note – The response characteristics in the Tx clock generation PLL in some devices have been known to drift during warm up. When this occurs, the drift appears to have a relatively fast time constant. If the card being tested demonstrates this effect, wait approximately 10 seconds before initiating the test.
4. Click SWEEP to begin the test. The test will take approximately 15 seconds to complete. Prior to stepping the S_j modulation, the analyzer initiates the test by generating a clean REF_CLK signal, and measures the edge density of the Tx output. The measured edge density is displayed continuously in real time in the upper right corner of the application software window. If the device is generating a normal compliance pattern without gaps, the transition density measurement should read approximately 73.4%.
5. At the completion of the test sweep, the measured loop bandwidth and peaking will be displayed. The software also compares these results against the compliance limits for a generation 1.1 device, and displays TEST PASSED or TEST FAILED at the top banner of the window.
6. To generate a test report hard copy, click FILE-PRINT from the top menu area in the software. A Test Information dialog box will first appear to allow the user to record information which will appear on the test report.



After entering the appropriate information, click OK. This brings up the standard Windows Print dialog box.



Select the printer of choice and click OK to generate a test report hard copy. To generate the test report and save as an HTML file for later printing, select FILE-PRINT TO FILE option from the top menu in the application.

This completes the PLL Loop Response test.