



PCI-SIG ENGINEERING CHANGE NOTICE

TITLE:	CLKREQ# dynamic protocol
DATE:	February 01, 2004
AFFECTED DOCUMENT:	PCI Express Mini Card, Release 1.0
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Part I

1. Summary of the Functional Changes

This change request proposes to add functionality to the existing CLKREQ# signal on the Mini Card interface. The purpose of this change is to define an enhanced PCI Express clock management protocol that will provide power saving benefit during periods when PCI Express links are idle.

2. Benefits as a Result of the Changes

This feature extension will enable the development of lower power modules and systems. The actual amount of power benefit will vary by application and implementation although the potential collective benefit across all of the applications potentially running in a single system is on the order of 100's of mW during periods of idle time on PCI Express links.

3. Assessment of the Impact

This feature is proposed as a new requirement of Mini Cards and an optional feature of host platforms. Timely inclusion of this new feature and promotion of its adoption in products is important in order to minimize the number of PCI Express-based Mini Cards that do not support dynamic clock management. Cards that do not support this feature are still compatible with the specification but may have the impact of inhibiting other cards installed in the same system from achieving the benefit (similar to the legacy PCI clock-run issue in CardBus PC Cards).

4. Analysis of the Hardware Implications

In order to implement, requires PCI Express end-point silicon to support the CLKREQ# signal generation either as a direct output of the silicon (supporting the protocol) or with signals (e.g. link status) that other components within the card's design can effectively derive the protocol to drive the CLKREQ# signal properly.

5. Analysis of the Software Implications

This protocol operates within the link state hardware of the end-point and relates to a hardware-based protocol between the card and the host's clock generation circuitry. This does not mean that software and/or BIOS may not be required in some systems designs in order to implement establishing the control link between the card and the clock generator. This is a system implementation detail for systems that wish to take advantage of this feature of the card.

Part II

Note: PCI Express Base Specification revision needs to be updated in this document to align with CLKREQ# features changes.

Change Section 3.2.4.1, page 28 as follows:

3.2.4.1. Reference Clock

The REFCLK+/REFCLK- signals are used to assist the synchronization of the card's PCI Express interface timing circuits. Availability of the reference clock at the card interface may be gated by the CLKREQ# signal as described in Section 3.2.4.2. When the reference clock is not available, it will be in the parked state. A parked state is when the clock is not being driven by a clock driver and both REFCLK+ and REFCLK- are pulled to ground by the ground termination resistors. Refer to the *PCI Express Card Electromechanical Specification* for more details on the functional and tolerance requirements for the reference clock signals.

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Change Section 3.2.4.2, page 28 as follows:

3.2.4.2. CLKREQ# Signal

The CLKREQ# signal is an open drain, active low signal that is driven low by the PCI Express Mini Card function to request that the PCI Express reference clock be available (active clock state) in order to allow the PCI Express interface to send/receive data. The operation of the CLKREQ# signal is determined by the state of the dynamic clock management enable bit in the Link Control Register (offset 010h). When disabled, the CLKREQ# signal shall be asserted at all times whenever power is applied to the card.

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Deleted: For this revision of the specification, this signal should always be asserted by PCI Express-based add-in cards and it is acceptable to simply tie this output low (using ground).

Whenever dynamic clock management is enabled and when a card stops driving CLKREQ# low, it indicates that the device is ready for the reference clock to transition from the active clock state to a parked (not available) clock state. Reference clocks are not guaranteed to be parked by the host system when CLKREQ# gets de-asserted and module designs shall be tolerant of an active reference clock even when CLKREQ# is de-asserted by the module.

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The card must drive this signal low during power up, whenever it is reset, and whenever it requires the reference clock to be in the active clock state. Whenever PERST# is asserted, including when the device is not in D0, CLKREQ# shall be asserted.

It is important to note that the PCI Express device must delay de-assertion of its CLKREQ# signal until it is ready for its reference clock to be parked. Also, the device must be able to assert its clock request signal, whether or not the reference clock is active or parked, when it needs to put its link back into the L0 link state. Finally, the device must be able to sense an electrical idle break on its up-stream-directed receive port and assert its clock request, whether or not the reference clock is active or parked.

The assertion and de-assertion of CLKREQ# are asynchronous with respect to the reference clock.

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Add-in cards that do not implement a PCI Express interface shall leave the CLKREQ# output unconnected on the card.

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CLKREQ# has additional electrical requirements over and above standard open drain signals that allow it to be shared between devices that are powered off and other devices that may be powered on. The additional requirements include careful circuit design to ensure that a voltage applied to the CLKREQ# signal network never causes damage to a component even if that particular component's power is not applied.

Additionally, the device must ensure that it does not pull CLKREQ# low unless CLKREQ# is being intentionally asserted in all cases, including when the related function is in D3_{cold}. This means that any component implementing CLKREQ# must be designed such that:

- Unpowered CLKREQ# output circuits are not damaged if a voltage is applied to them from other powered "wire-ORed" sources of CLKREQ#.
- When power is removed from its CLKREQ# generation logic, the unpowered output does *not* present a low impedance path to ground or any other voltage.

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These additional requirements ensure that the CLKREQ# signal network continues to function properly when a mixture of powered and unpowered components have their CLKREQ# outputs wire-ORed together. It is important to note that most commonly available open drain, and tri-state buffer circuit designs used "as is" do not satisfy the additional circuit design requirements for CLKREQ#.

Add Section 3.2.4.2.1 as follows:

3.2.4.2.1. Power-up requirements

CLKREQ# is asserted in response to PERST# assertion. On power up, CLKREQ# must be asserted by a PCI Express device within a delay (T_{PVCRL}) from the power rails achieving specified operating limits and PERST# assertion. This delay is to allow adequate time for the power to stabilize on the card and certain system functions to start prior to the card starting up. CLKREQ# may not be de-asserted while PERST# is asserted.

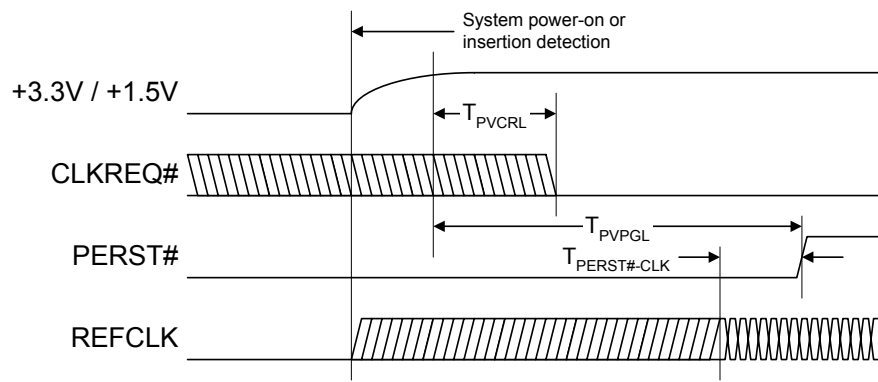


Figure 3-1: Power-Up CLKREQ# Timing

Table 3-1a: Power-Up CLKREQ# Timings

<u>Symbol</u>	<u>Parameter</u>	<u>Min</u>	<u>Max</u>	<u>Units</u>
<u>T_{PVCRL}</u>	<u>Power Valid to CLKREQ# output active</u>		<u>100</u>	<u>μs</u>
<u>T_{PVPL}</u>	<u>Power Valid to PERST# input inactive</u>	<u>1</u>		<u>ms</u>
<u>T_{PERST#-CLK}</u>	<u>REFCLK stable before PERST# inactive</u>	<u>100</u>		<u>μs</u>

The system is required to have the reference clock for a PCI Express device in the parked clock state prior to device power-up. The state of the reference clock is undefined during device power-up, but it must be in the active clock state for a setup time T_{PERST#-CLK} prior to PERST# de-assertion.

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Add Section 3.2.4.2.2 as follows:

3.2.4.2.2. Dynamic clock control

After a PCI Express device has powered up and whenever its upstream link enters the L1 link state, it shall allow its reference clock to be turned off (put into the parked clock state). To accomplish this, the device de-asserts CLKREQ# (high) and it must allow that the reference clock will transition to the parked clock state within a delay (T_{CRloff}).

To exit L1, the device must assert CLKREQ# (low) to re-enable the reference clock. After the device asserts CLKREQ# (low) it must allow that the reference clock will continue to be in the parked clock state for a delay (T_{CRlon}) before transitioning to the active clock state. The time that it takes for the device to assert CLKREQ# and for the system to return the reference clock to the active clock state are serialized with respect to the remainder of L1 recovery. This time must be taken into account when the device is reporting its L1 exit latency.

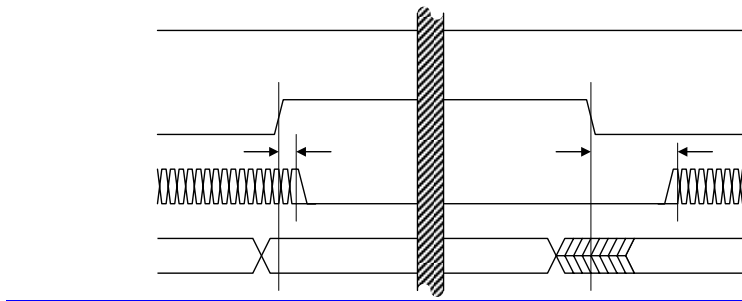


Figure 3-2: CLKREQ# Clock Control Timings

All links attached to a PCI Express device must complete a transition to the *L1,Idle* state before the device can de-assert CLKREQ#. The device must assert CLKREQ# when it detects an electrical idle break on any receiver port. The device must assert CLKREQ# at the same time it breaks electrical idle on any of its transmitter ports in order to minimize *L1* exit latency.

Table 3-1b: CLKREQ# Clock Control Timings

<u>Symbol</u>	<u>Parameter</u>	<u>Min</u>	<u>Max</u>	<u>Units</u>
<u>T_{CRHoff}</u>	<u>CLKREQ# de-asserted high to clock parked</u>	<u>0</u>		<u>ns</u>
<u>T_{CRLon}</u>	<u>CLKREQ# asserted low to clock active</u>		<u>400</u>	<u>ns</u>

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There is no maximum specification for T_{CRHoff} and no minimum specification for T_{CRLon}. This means that the system is not required to implement reference clock parking or that the implementation may not always act on a device de-asserting CLKREQ#.

A device should also de-assert CLKREQ# when its link is in *L2* or *L3*, much as it does during *L1*.

Add Section 3.2.4.2.3 as follows:

3.2.4.2.3. Clock request support reporting and enabling

Support for the CLKREQ# dynamic clock protocol should be reported using bit 18 in the PCI Express link capabilities register (offset 0C4h). System software should enable this feature if both device and platform support dynamic clock management functionality using bit 8 of the Link Control Register (offset 010h). See the *PCI Express Base Specification 1.1* (or later) for more information regarding these bits.

Change Section 3.2.4.3, page 28 as follows:

3.2.4.3. PERST# Signal

The PERST# signal is de-asserted to indicate when the system power sources are within their specified voltage tolerance and are stable. PERST# should be used to initialize the card functions once power sources stabilize. PERST# is asserted when power is switched off and also can be used by the system to force a hardware reset on the card. The system may also use PERST# to cause a warm reset of the add-in card. Refer to the *PCI Express Card Electromechanical Specification* for more details on the functional requirements for the PERST# signal.

Deleted: The operation of the CLKREQ# signal is impacted by PERST# as described in Section 3.2.4.2.