



## PCI-SIG ENGINEERING CHANGE NOTICE

<b>TITLE:</b>	Removing Downshift Reference from CEM Spec
<b>DATE:</b>	Jan. 16, 2005
<b>AFFECTED DOCUMENT:</b>	PCI Express CEM Specification 1.0a, 1.1
<b>SPONSOR:</b>	Yun Ling, Intel Corporation

### **Part I**

#### **1. Summary of the Functional Changes**

Remove the definition of and all references to downshifting in the CEM spec and treat connector wiring entirely as an OEM implementation issue. The spec then neither explicitly endorses nor prohibits downshifting.

#### **2. Benefits as a Result of the Changes**

This will untie PCI SIG and the CEM spec from the downshifting or connector short-wiring practice. OEMs who chose to short-wire a connector will no longer have a spec non-compliance issue, but they must manage any potential downshifting-related issue themselves.

#### **3. Assessment of the Impact**

The specification changes are minor and primarily contained just to Section 6.3. There are no other specification impacts anticipated.

#### **4. Analysis of the Hardware Implications**

There are no impacts to existing silicon and other components. The primary specification changes only remove all references to downshifting. All additional functionality described in this ECR is optional for all components compliant with the PCIe 1.0a and 1.1 CEM specifications.

#### **5. Analysis of the Software Implications**

There are no impacts to software as the changes are confined entirely to the CEM specification. Full interoperability with existing software is maintained.

## **Part II**

The specification changes are confined to Section 1.1 Terms and Definitions and Section 6.3 Card Interoperability. The change in Section 1.1 is to remove the downshifting definition. The primary changes are for Section 6.3.

**The current specification text is as follows:**

### **6.3 Card Interoperability**

PCI Express cards and slots will exist with a variety of Link widths. The interoperability of cards and slots is summarized in Table 6-2.

**Table 6-2: Card Interoperability**

<b>Slot \ Card</b>	<b>x1</b>	<b>X4</b>	<b>x8</b>	<b>x16</b>
<b>x1</b>	Required	Required	Required	Required
<b>x4</b>	No	Required	Allowed	Allowed
<b>x8</b>	No	No	Required	Allowed
<b>x16</b>	No	No	No	Required

Note that the shaded area above the diagonal of Table 6-2 represents up-plugging, while the area below the diagonal represents down-plugging. The following points should be noted:

- Down-plugging, i.e., plugging a larger Link card into a smaller Link connector, is not allowed and is physically prevented.
- Up-plugging, i.e., plugging a smaller Link card into a larger Link connector, is fully allowed.
- Down-shifting, which is defined as plugging a PCI Express card into a connector that is not fully routed for all of the PCI Express lanes, in general is not allowed. The exception is the x8 connector which the system designer may choose to route only the first four PCI Express lanes. A x8 card must function as a x4 card in this scenario.

**The modified specification text in section 6.3 is as follows:**

### **6.3 Card Interoperability**

PCI Express cards and connectors exist with a variety of Link widths. The interoperability of cards and connectors is summarized in Table 6-2.

**Table 6-2: Card Interoperability**

<b>Connector Card</b>	<b>x1</b>	<b>x4</b>	<b>x8</b>	<b>x16</b>
x1	Required	Required	Required	Required
x4	No	Required	Allowed	Allowed
x8	No	No	Required	Allowed
x16	No	No	No	Required

Note that the connectors here refer to the receptacle connectors mounted on a system board, as defined in Chapter 5. The shaded area above the diagonal of Table 6-2 represents up-plugging, while the area below the diagonal represents down-plugging. The following points should be noted:

- Down-plugging, i.e., plugging a larger edge size card into a smaller connector, is not allowed and is physically prevented.
- Up-plugging, i.e., plugging a smaller edge size card into a larger connector, is allowed.
- A x8 PCI Express Add-in Card must be able to negotiate and operate as a x4 Card
- A system with a x8 connector may route only the first four PCI Express lanes to the connector.
- The upstream PCI Express components on a system board may negotiate and operate with smaller link width cards. For example, components may support a x1, x4, or x8 card in a x16-lane connector.