PCI-SIG ENGINEERING CHANGE NOTICE

TITLE:	Input Power and Voltage Tolerance
DATE:	May 16, 2005
AFFECTED DOCUMENT:	PCI Express Mini CEM, Rev 1.1
SPONSOR:	Pratik Mehta; Dell

Part I

1. Summary of the Functional Changes

Changes are proposed that would serve to align the Mini CEM specification input power requirements with that of the WFF CEM specification.

Change to increase current limit

1. Increse the maximum current allowed to 2,750 / 1,100 (Peak / Normal)
2. Merge +3.3V and +3.3Vaux into +3.3Vaux
3. Add two ground and two +3.3Vaux pins. (Total of 5 +3.3Vaux pins)

2. Benefits as a Result of the Changes

This will align the mini-CEM with the WFF CEM to allow common hardware architectures in the different form factors.

3. Assessment of the Impact

Should ease costs associated with delivering similar products in both form-factors.

4. Analysis of the Hardware Implications

The additional power and ground pins will enable higher power cards that are expected in future, such as WWAN. These benefits have been discussed during the development discussions in the WFF WG. These changes brings the Mini CEM in alignment with WFF work, and allows more efficient operations for WWAN.

5. Analysis of the Software Implications

N/A

Part II

Detailed Description of the change

Change Table 3.1, page 25 as follows:

Table 3-1: PCI Express Mini Card System Interface Signals

Signal Group	Signal	Direction	Description
Power	+3.3Vaux (5 pins)		3.3 V source
	+1.5V (3 pins)		1.5 V source
	GND (14 pins)		Return current path
PCI Express	PETp0, PETn0 PERp0, PERn0	Input/Output	PCI Express x1 data interface: one differential transmit pair and one differential receive pair
	REFCLK+, REFCLK–	Input	PCI Express differential reference clock (100 MHz)
Universal Serial Bus (USB)	USB_D+, USB_D–	Input/Output	USB serial data interface compliant to the USB 2.0 specification
Auxiliary Signals (3.3V Compliant)	PERST#	Input	Functional reset to the card
	CLKREQ#	Output	Reference clock request signal
	WAKE#	Output	Open Drain active Low signal. This signal is used to request that the system return from a sleep/suspended state to service a function initiated wake event.
	SMB_DATA	Input/Output	SMBus data signal compliant to the SMBus 2.0 specification
	SMB_CLK	Input	SMBus clock signal compliant to the SMBus 2.0 specification
Communications Specific Signals	LED_WPAN#, LED_WLAN#, LED_WWAN#	Output	Open Drain, active low signals. These signals are used to allow the PCI Express Mini Card add-in card to provide status indicators via LED devices that will be provided by the system.
	W_DISABLE#	Input	Active low signal. This signal is used by the system to disable radio operation on add-in cards that implement radio frequency applications. When implemented, this signal requires a pull-up resistor on the card.

Deleted: 2

Deleted: Primary

Deleted: +3.3Vaux (1 pin)

Deleted: Auxiliary 3.3 V source

Deleted: Primary

Deleted: 12

Signal Group	Signal	Direction	Description
User Identity Module (UIM) Signals	UIM_PWR (1 pin)	Output	Power source for the UIM. Compliant to the ISO/IEC 7816-3 specification (VCC).
	UIM_RESET	Output	UIM reset signal. Compliant to the ISO/IEC 7816-3 specification (RST).
	UIM_CLK	Output	UIM clock signal. Compliant to the ISO/IEC 7816-3 specification (CLK).
	UIM_VPP	Output	Variable supply voltage (e.g., programming voltage) for class A devices. Refer to ISO/IEC 7816-3 for operating class definitions. This signal is reserved for future use for devices of other classes. Compliant to the ISO/IEC 7816-3 specification (VPP).
	UIM_DATA	Input/Output	UIM data signal. Compliant to the ISO/IEC 7816-3 specification (I/O).

3.2.1. Power Sources and Grounds

PCI Express Mini Card provides two power sources: one at 3.3Vaux (3.3Vaux) and one at 1.5V (+1.5V). The auxiliary voltage source +3.3Vaux may be the only supply voltage available during the system's stand-by/suspend state to support wake event processing on the communications card. The 1.5V may or may not be present in the low power state.

Deleted: three
Deleted: two
Deleted: +3.3V
Deleted: and
Deleted: (
Deleted:)

3.2.4. Auxiliary Signals

… The optional low speed signals are defined to use the +3.3Vaux supply, as they are the lowest common voltage available. ….

Deleted: +3.3V or
Deleted: ies

3.2.4.4. WAKE# Signal

… If the wakeup process is used, the +3.3Vaux supply must be present and used for this function. …

3.2.5.2. W_DISABLE# Signal

… The system is required to assure that W_DISABLE# be in a deterministic state (asserted or deasserted) whenever power is applied to the add-in; i.e., +3.3Vaux is present. …

Deleted: whenever either
Deleted:
Deleted: +3.3V or

Change Table 3-6, page 36 as follows:

Table 3-6: System Connector Pin-out

Pin #	Name	Pin #	Name
51	Reserved	52	+3.3Vaux
49	Reserved	50	GND
47	Reserved	48	+1.5V
45	Reserved	46	LED_WPAN#
43	GND	44	LED_WLAN#
41	+3.3Vaux	42	LED_WWAN#
39	+3.3Vaux	40	GND
37	GND	38	USB_D+
35	GND	36	USB_D-
33	PETp0	34	GND
31	PETn0	32	SMB_DATA
29	GND	30	SMB_CLK
27	GND	28	+1.5V
25	PERp0	26	GND
23	PERn0	24	+3.3Vaux
21	GND	22	PERST#
19	Reserved*** (UIM_C4)	20	W_DISABLE#
17	Reserved*** (UIM_C8)	18	GND
Mechanical Key			
15	GND	16	UIM_VPP
13	REFCLK+	14	UIM_RESET
11	REFCLK-	12	UIM_CLK
9	GND	10	UIM_DATA
7	CLKREQ#	8	UIM_PWR
5	COEX2	6	1.5V
3	COEX1	4	GND
1	WAKE#	2	3.3Vaux

*** Reserved for future UIM interface (if needed)

Deleted: *
Deleted: *
Deleted: *
Deleted: *
Deleted: Reserved*
Deleted: Reserved*
Deleted: Reserved*
Deleted: Reserved*
Deleted: * Reserved for future second PCI Express Lane (if needed)

3.4.2. Power

PCI Express Mini Card has two defined power rails: +3.3Vaux, and +1.5V. Table 3-8 lists the voltage tolerances and power ratings for each PCI Express Mini Card slot implemented in a system.

Change Table 3-8, page 40 as follows.

Table 3-8: Power Ratings

Power Rail	Voltage Tollerance	D0-D2 D3hot Power[1]		D3cold Power[2,3]	
		Peak (max) mA	Normal (max) mA	Peak (max) mA	Normal (max) mA
3.3Vaux	+/-9%	2,750	1,100	2,750 (wake enabled)	250 (wake enable) 5 (no wake enable)
+1.5V	+/-5%	500	375	N/A	N/A

1 For USB: power states greater than Bus Suspend.
2 For USB: Wake enabled is USB Remote wakeup-Enabled and No Wake enabled is USB Remote wakeup-Disabled.
3 This D3 current limit only applies when the +1.5V voltage source is not available; i.e., the card is in a low power D3 state.

Definitions:
Peak – The highest averaged current value over any 100-microsecond period
Normal – The highest averaged current value over any 1-second period

Note: For Peak, the value of "100-microsecond period" was derived as follows: The period of time that the current is to be measured and averaged over must be less than a single GPRS slot time. This enables measurement of the average peak current within a single GPRS slot. There are 4.6 milliseconds/GPRS frame and 8 slots per GPRS frame = 575 microseconds/slot. The 100 microsecond period < 575 microsecond period.

The operation of the +3.3Vaux power source shall conform to the *PCI Bus Power Management Interface Specification* and the *Advanced Configuration and Power Interface (ACPI) Specification*, except as otherwise specified by this document. If the host does not support wake from D3, +3.3Vaux may be removed by the host when +1.5V is removed.

Deleted: three
Deleted: +3.3V,
Deleted: Primary
Formatted: Superscript
Deleted: Auxiliary
Deleted: *
Formatted: Superscript
Formatted Table
Formatted: Italian (Italy)
Deleted: +3.3V
Deleted: +/-9%
Deleted: 1,000
Deleted: 750
Deleted: N/A
Deleted: 330
Deleted: 250
Deleted: <#>When available, the total power drawn by a PCI Express MIni Card function for the sum of +3.3V and +3.3Vaux shall not exceed 750 mA (Normal max) and, 1,000 mA (Peak max).¶
Formatted: Indent: Left: 0.25"
Formatted: Bullets and Numbering
Formatted: Indent: Left: 0.25"
Deleted: auxiliary
Deleted: primary +3.3V and
Deleted: s are
Deleted: 10-millisecond
Formatted: Indent: Left: 0.5"
Formatted: Indent: Left: 1"
Deleted: +3.3Vaux and +3.3V must be isolated power planes within the PCI Express Mini Card add-in card. The card cannot connect the +3.3Vaux to +3.3V.¶
Deleted: +3.3V and
Deleted: s