

**PCI**



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**PCI Express™  
Slots and Add-in Cards**

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**Chairman, PCI Express Working Group**

**PCI-SIG**

# Agenda

- **Highlights**
- **Add-in Card form factors**
- **Connector**
- **Conventional PCB routing technology**
- **Power/thermal specs**
- **Interoperability**
- **Auxiliary interfaces**
- **Board layout design guidelines**
- **Summary**

# Highlights

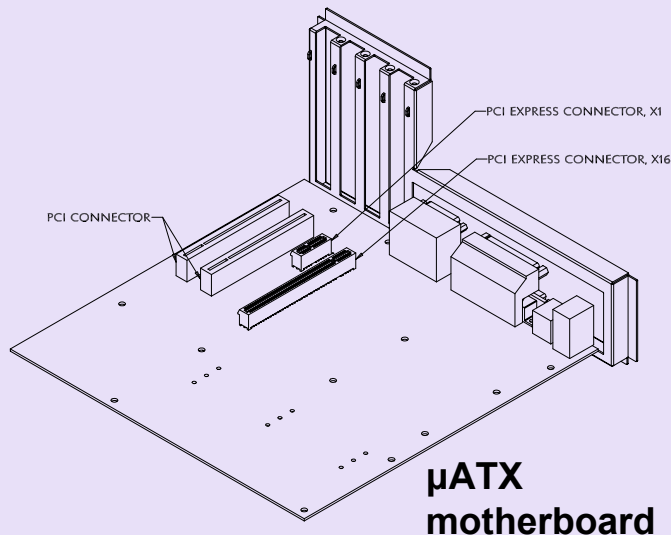
- **Fits in Desktop and Server Infrastructure**
- **Features for Card Retention**
- **Simplified Power Delivery**
- **Support for System Interface Signals**
- **Routing in 4 Layer Motherboards**

# Fits in Desktop Infrastructure



**Uses Existing ATX Chassis**  
Does not require chassis changes

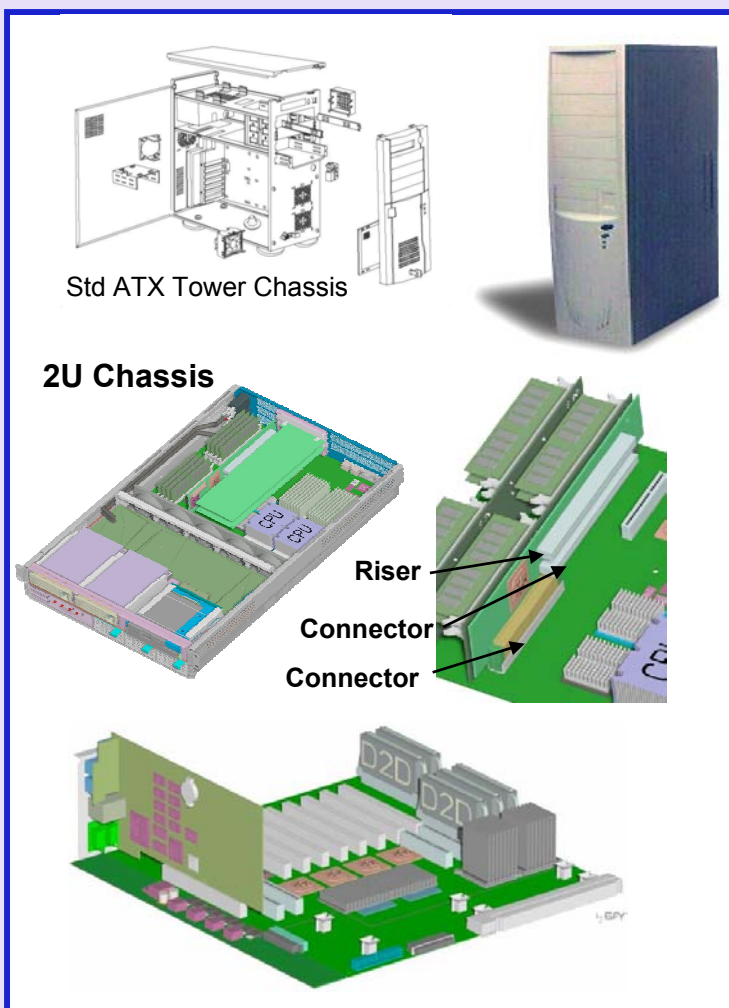
**Can Be Implemented with ATX/ $\mu$ ATX Motherboards**



**Capable of Transition with PCI**

**Both PCI and PCI Express can be implemented together on motherboard**

# Fits into Existing Server Applications



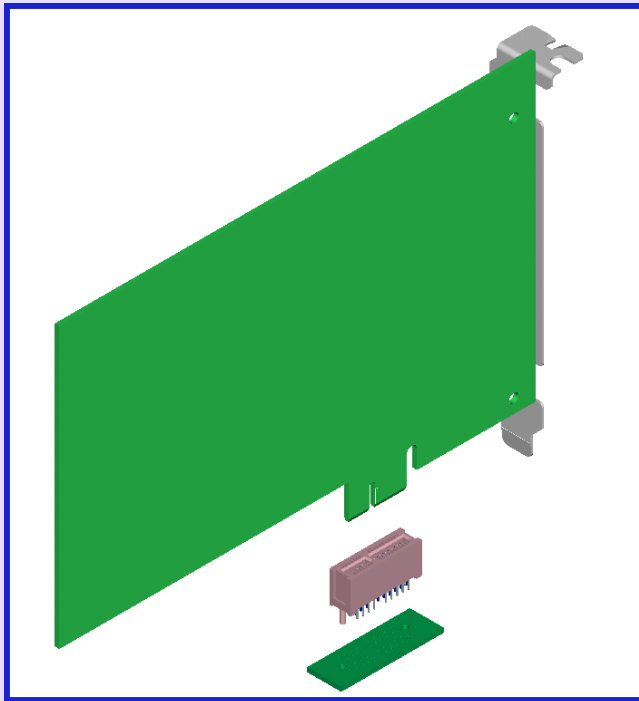
**Uses Existing Server Chassis**  
Does not require chassis changes

**Can Be Implemented in Rack Mount Server Chassis**

Can be routed through two connectors and riser card

**Capable of Transition with PCI**

# Simple Add-in Card Design



**Follows PCI Card form factors**

**Standard Height Cards, 4.20" (106.7mm)**

**Low Profile Cards, 2.536" (64.4mm)**

**Half Length Cards, 6.6" (167.65mm)**

**Full Length Cards, 12.283" (312mm)**

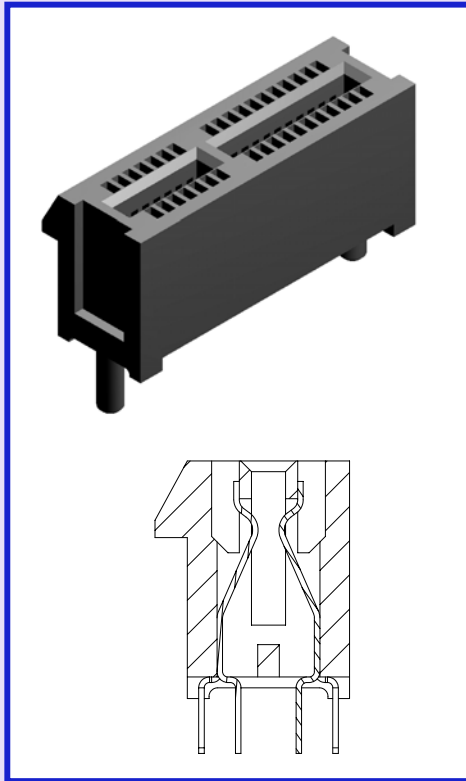
**Uses PCI I/O Bracket**

**PCI Express Is Optimized for Cost**

# Add-in Card Size Exceptions

- **Standard height x1 cards are limited to half-length (6.6") for desktop applications**
  - ✓ **Push towards small form factor systems**
  - ✓ **10W power limit**
- **For server I/O needs there is allowance for a 25W, standard height x1 card that **MUST** be greater or equal to 7.0" but less than or equal to full length**

# Low Cost Edge Card Connector



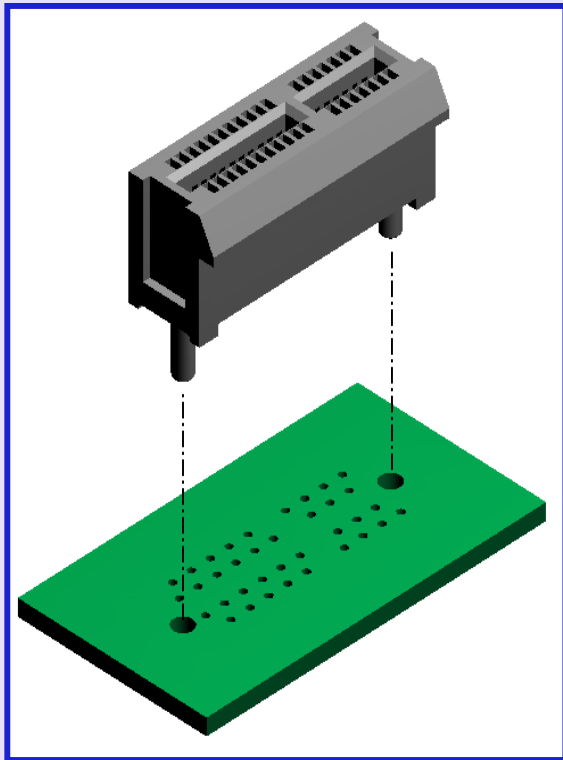
**x1 connector 36 pins vs.  
PCI 120 pins**

**Simple Single Level Contacts**

**1mm Contact Spacing**

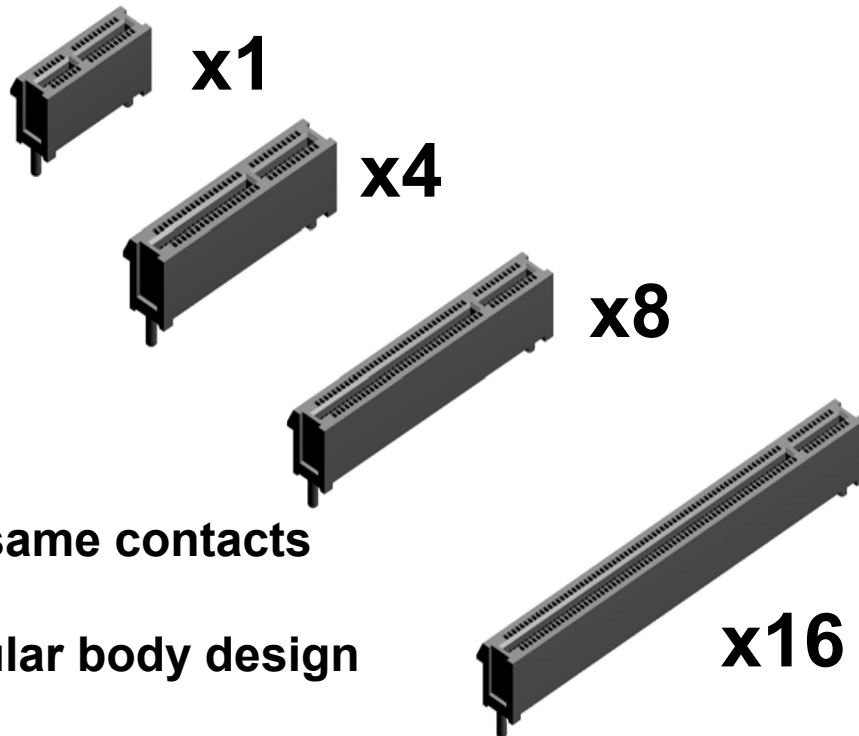
**Low Cost Connector Assembly**

# Through Hole Design Capability



**Simple through-hole  
design supports low  
cost board assembly  
processes**

# Scalable Connector Design



Use same contacts

Modular body design

Use same connector  
manufacturing process

**Scalable Design  
allows connectors  
from x1 to x16 to be  
easily designed**

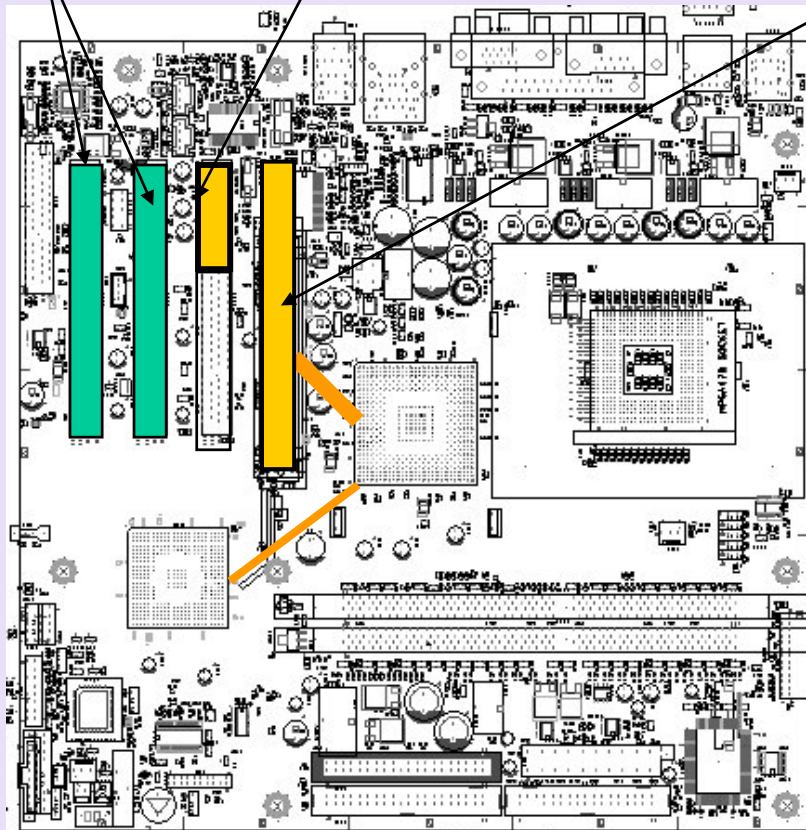
**Smaller link-width  
cards can plug  
into larger link-  
width connectors**

# Routing in 4-Layer Motherboards

PCI  
Connectors

PCI Express x1 connector  
(4 times PCI performance)

PCI Express x16 connector  
(64 times PCI performance)



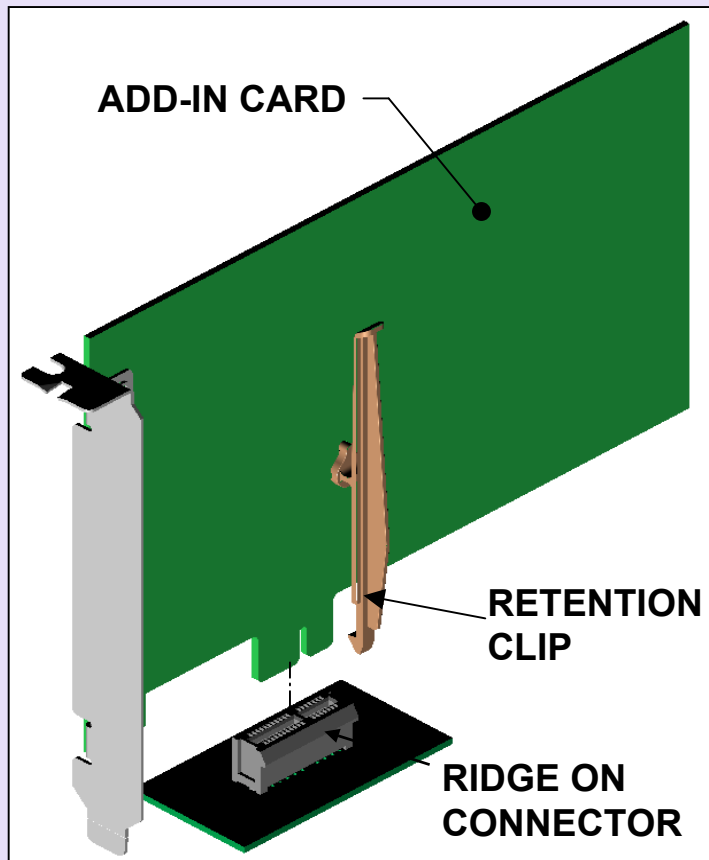
**PCI Express layout and  
connectors can be routed  
in 4 Layers**

**Flexibility in routing PCI  
Express and PCI  
connectors on the  
same board**

**Smaller connectors  
provide more room for  
routing and components**

**μATX 4 Layer, P4 Motherboard**

# Support for Add-in Card Retention



The connector has a ridge molded into the housing to enable a number of card retention schemes to be implemented.

Graphics add-in card designs **MUST** have a provision for a retention clip.

# Simplified Power Delivery

<i>Power Rail</i>	<i>x1 connector; 10W limit (DT)</i>	<i>x1 connector (server I/O), x4/x8 connector, x16 connector (I/O); 25W limit</i>	<i>x16 connector (Gfx); 40W limit</i>
<b>+3.3V ±9%</b>	<b>3A max</b>	<b>3A max</b>	<b>3A max</b>
<b>+12V ±8%</b>	<b>0.5A max</b>	<b>2.1A max</b>	<b>3.3A max</b>
<b>+3.3Vaux ±9%</b>	<b>375mA max</b>	<b>375mA max</b>	<b>375mA max</b>

**Note:**

- **3.3Vaux max current is 375mA when the add-in card is Wake enabled and 20mA when Wake disabled.**

**Compared to PCI:**

- **Additional power from 12v rail**
- **+5V, -12V requirements are eliminated**

# Power Rules

- **System MUST provide +12V and +3.3V rails to ALL PCI Express slots in a chassis**
- **Systems may optionally provide +3.3Vaux but if supplied it MUST be provided to all PCI Express slots in a chassis**
- **If the platform supports the WAKE# signal then it MUST provide it and +3.3Vaux to all PCI Express slots in chassis**
- **Capacitive load rules:**
  - ✓ **+12V rail: 300 $\mu$ F @ 10W; 1000 $\mu$ F @ 25W; 2000 $\mu$ F @ 40W**
  - ✓ **+3.3V rail: 1000 $\mu$ F**
  - ✓ **+3.3Vaux rail: 150 $\mu$ F**

## Power Rules (Continued)

- **Current slew rate: 0.1A/ $\mu$ s**
- **All x1 add-in cards must power up at a maximum of 10W; once configured as a High Power device, if applicable, a card can consume up to 25W**
- **All x16 add-in cards must power up at a maximum of 25W; once configured as a High Power device, if applicable, a graphics card can consume up to 40W**

# Add-in Card Interoperability

Slot Card	x1	x4	x8	x16
x1	Yes	Yes	Yes	Yes
x4	No	Yes	Yes	Yes
x8	No	No	Yes	Yes
x16	No	No	No	Yes

- **Up-plugging:** Plugging a smaller link card into a larger link connector. Fully allowed and must be fully supported.
- **Down-plugging:** Plugging a larger link card into a smaller link connector. Not allowed and is physically prevented.
- **Down-shifting:** Plugging a card into a connector that is not fully routed for all of the lanes. In general, this is not allowed. The exception is the x8 connector which the system designer may choose to route only the first four lanes. A x8 card functions as a x4 card in this scenario.

# Support for System Interface Signals

- **Connector supports common interface signals for easy system implementation:**
  - ✓ **Reference Clock**
  - ✓ **SMBus**
  - ✓ **Power Good**
  - ✓ **Wake**
  - ✓ **JTAG**
  - ✓ **Card Presence Detect**

# Reference Clock (REFCLK+, REFCLK-)

- Differential pair
- Nominal frequency of 100MHz ( $\pm 300$ ppm)
- Point-to-point connection between each PCI Express connector and the clock source
- Within each differential pair the PCB trace lengths must be within 0.005"
- Spread Spectrum support is optional

# SMBus (SMBCLK, SMBDAT)

- Provides a simple control bus for applications such as ASF and IPMI
- Use by the system or add-in card is **OPTIONAL!**
- If supported by the system it **MUST:**
  - ✓ Provide SMBus connections to **ALL** slots in a chassis
  - ✓ Provide bus pull-ups (active or passive) to +3.3Vaux, if present, or +3.3V if 3.3Vaux is not provided to the slots
  - ✓ Support SMBus 2.0 per its spec (e.g. ARP)
- If supported by the add-in card it **MUST:**
  - ✓ Adhere to the SMBus 2.0 specs (e.g. ARP, electrical rules)

# Power Good (PWRGD)

- **Provided by the system**
- **Asserted (high) 100ms after the power rails have reached their spec levels**
- **Reference Clock must be stable when PWRGD is asserted**
- **All PCI Express functions held in reset whenever PWRGD is deasserted**

# Wake (WAKE#)

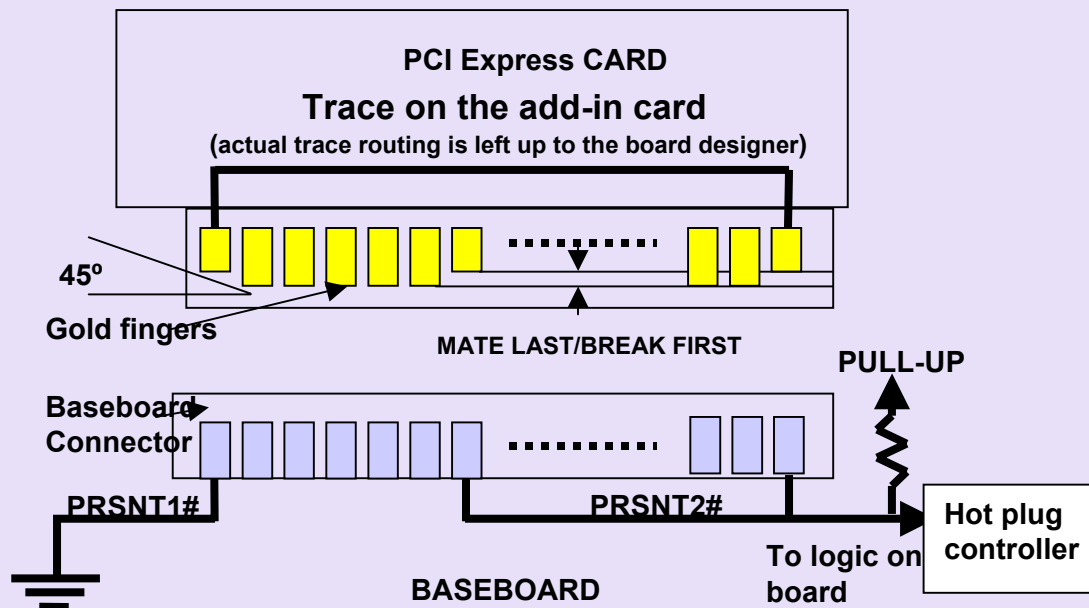
- Open drain, active low, asynchronous to any system clock
- Use by the system or add-in card is **OPTIONAL!**
- Reduced function compared to PCI's PME#
  - ✓ When WAKE# is asserted by a device it reactivates the PCI Express link hierarchy's main power and reference clocks.
  - ✓ Do NOT connect it to the system's PME# interrupt mechanism!!!
- System must wire-OR the WAKE# connections from all PCI Express slots in a chassis as well as provide a pull-up resistor biased to +3.3Vaux

# JTAG

- **Five pins dedicated for JTAG**
  - ✓ TCK, TMS, TDI, TDO, TRST#
- **Use by the system or add-in card is OPTIONAL!**
  - ✓ **If the system does not support JTAG on the connector then:**
    - TMS and TDI must be independently bused and pulled up, each with ~5K $\Omega$  resistors.
    - TRST# and TCK must independently bused and pulled down, each with ~5K $\Omega$  resistors.
    - TDO must be left open
- **Refer to IEEE Standard 1149.1 for a complete description as well as AC & DC parameters**

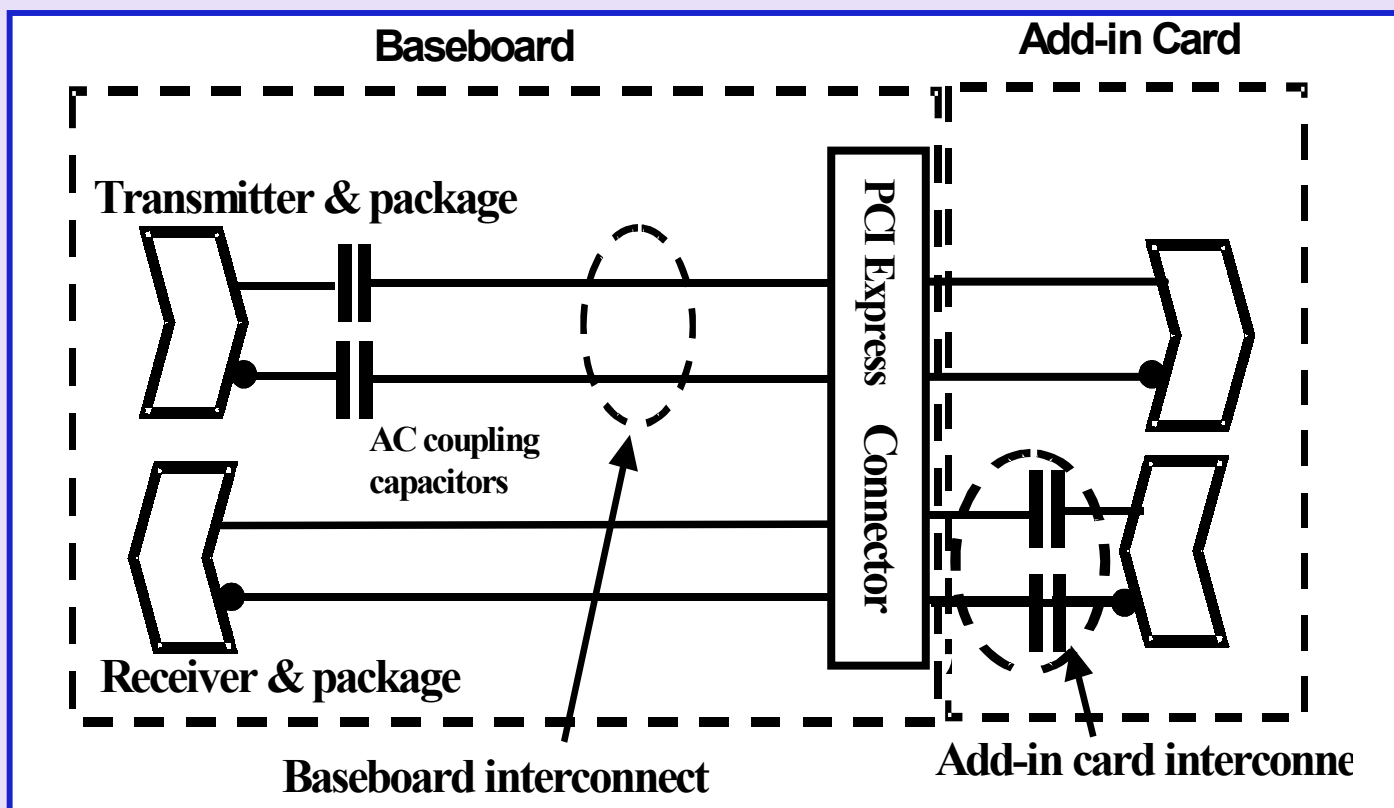
# Card Presence Detect

- Supports the hot plug solution and is required of ALL add-in cards
- System use is optional for non-hot plug solutions
- There are multiple PRSNT2# pins on the connector
  - ✓ System buses them together
  - ✓ Add-in card connects PRSNT1# to the FURTHEST PRSNT2# pin on its connector



# Board Layout Design Guidelines

## Link “schematic” diagram



# Add-in Card Layout Design Guidelines

- **AC Coupling Capacitors**
  - ✓ Must be located at the PCI Express transmitter end
  - ✓ Use 0603 or 0402 SMT component
  - ✓ Suggested value 75nF to 500nF
- **As a rule of thumb trace lengths should be no greater than 4” from the top of the gold fingers on the card edge to the PCI Express device**
- **Lane to lane trace length skew can be up to 2” (5 mil wide on FR4)**
- **Trace length skew within a differential pair should be < 5 mils**
- **Routing guidelines**
  - ✓ 5/5 trace/space within a differential pair
  - ✓ 20 mil space between pairs
  - ✓ Tx traces on component side
  - ✓ Rx traces on solder side

# Baseboard Layout Design Guidelines

- **AC Coupling Capacitors**
  - ✓ Must be located at the PCI Express transmitter end
  - ✓ Use 0603 or 0402 SMT component
  - ✓ Suggested value 75nF to 500nF
- **As a rule of thumb trace lengths should be no greater than 12" between the PCI Express device and the connector pins**
  - ✓ Highly dependent to routing topology used (stripline or microstrip)
- **Lane to lane trace length skew can be up to 7" (5 mil wide on FR4)**

# Baseboard Layout Design Guidelines (Continued)

- Trace length skew within a differential pair should be < 10 mils
- Electrical losses due to riser interconnect, if applicable, must be accounted for in the baseboard budget
- Routing guidelines
  - ✓ 5/5 trace/space within a differential pair
  - ✓ 20 mil space between pairs
  - ✓ Tx traces on component side
  - ✓ Rx traces on solder side

# Summary

- **PCI Express is Optimized for Cost**
  - ✓ Cost-effective for migration into commodity infrastructure
  - ✓ Replaces PCI over time with 15+ years of life
- **PCI Express is Easy to Implement**
  - ✓ Leverages existing form factors and standards
  - ✓ Transition with existing PCI form factors

# Call to Action

- **Prepare your product roadmaps to intercept first launch**
- **Utilize the PCI-SIG for specifications and support**

**Thank you for attending the 2002 PCI-SIG  
Developers Conference Tour and your  
continued efforts in advancing PCI I/O  
Technology!**

**Visit [www.pcisig.com](http://www.pcisig.com) for additional information  
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