

PCI

SIGTM

PCI ExpressTM Software and Configuration Model

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PCI Express Software and Configuration Model

- PCI Compatibility
 - ✓ Legacy-free migration guidelines
- PCI Express Topology
 - ✓ PCI Express to PCI Device Mapping
- PCI Express Capability Structure
- Hot-Plug
- PME Delivery
- Extended Configuration Model
- Advanced Features
 - ✓ Advanced Error Reporting
 - ✓ Isochrony/QoS Support through Traffic Classes / Virtual Channels



PCI Compatibility

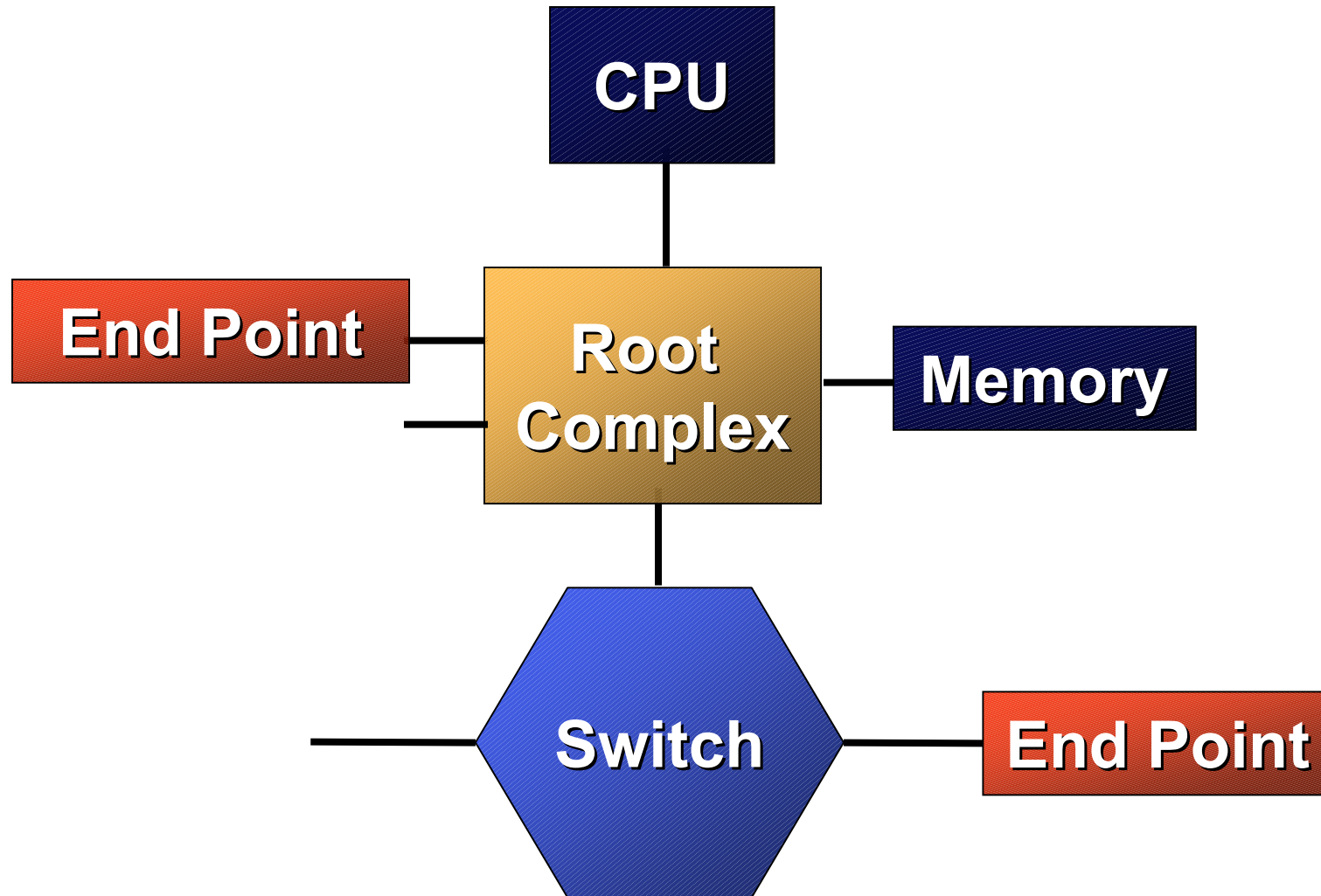
- PCI Configuration Mechanism #1 supported
- PCI compatible configuration header
 - ✓ Configuration space locations at offsets 0x00 to 0x3F work as in PCI
 - ✓ PCI compatible device enumeration and resource allocation
- Power management through PCI PM capability
 - ✓ PME supported using in-band messaging
- PCI compatible in-band INTx legacy interrupt emulation
- MSI support
 - ✓ MSI is the native interrupt mechanism in PCI Express



Legacy Free Migration Guidelines

- Use MSI for device interrupts
 - ✓ MSI support is required for PCI Express
- IO space permitted only for “Legacy Devices”
 - ✓ Alias I/O resources if required through MMIO
 - Allows I/O decode to be turned off at run-time
 - ✓ Devices needing I/O at run-time **MUST** indicate “Legacy Device”
 - “Legacy Devices” may not be supported in future versions of spec
 - ✓ Legacy I/O space support for option ROM boot
 - Firmware assigns I/O BARs to required boot devices
 - Operating system only assigns I/O space to devices that indicate “Legacy Device” type
 - I/O bars of other devices may be closed by OS

Simple PCI Express System

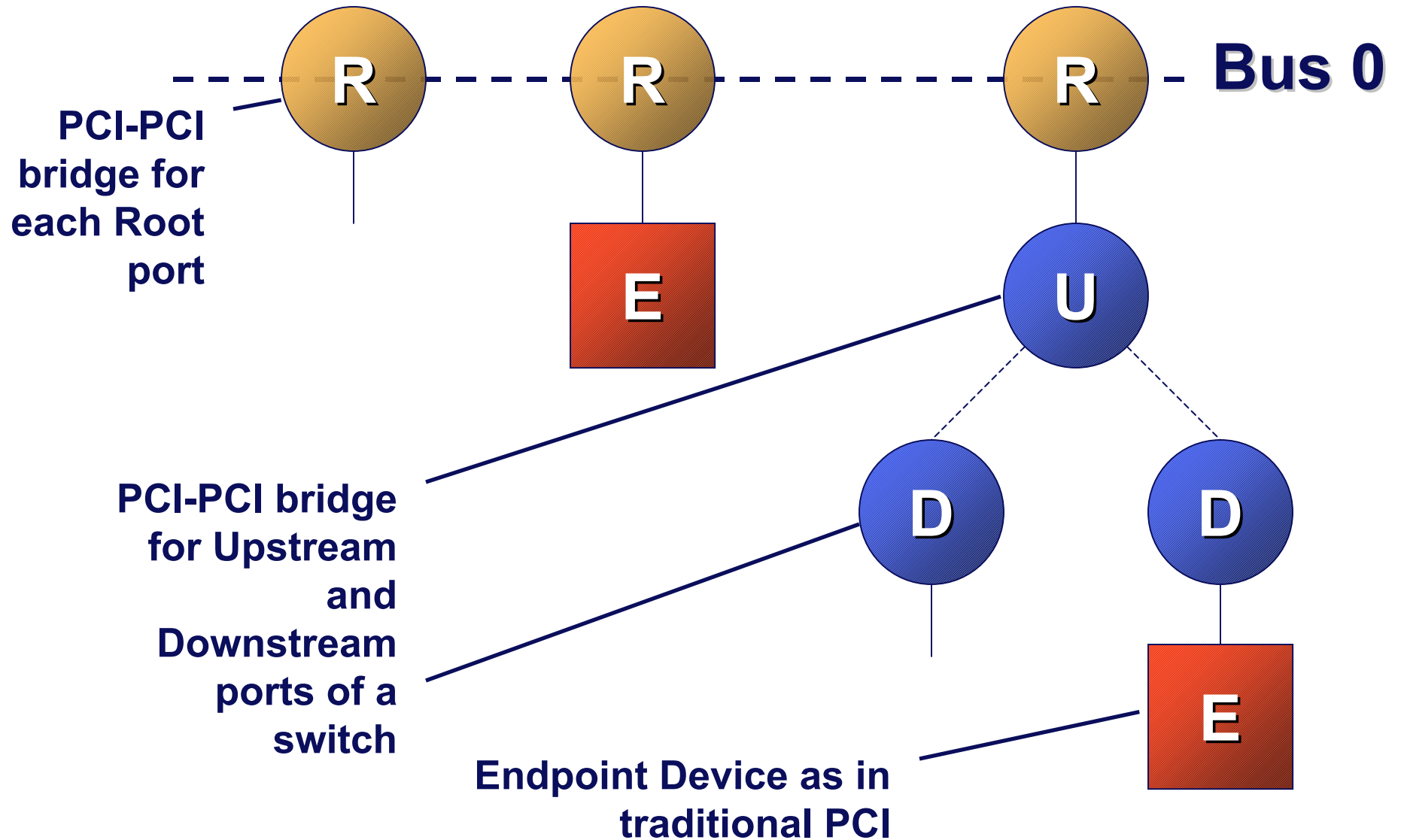




Mapping PCI Express to PCI Configuration Model

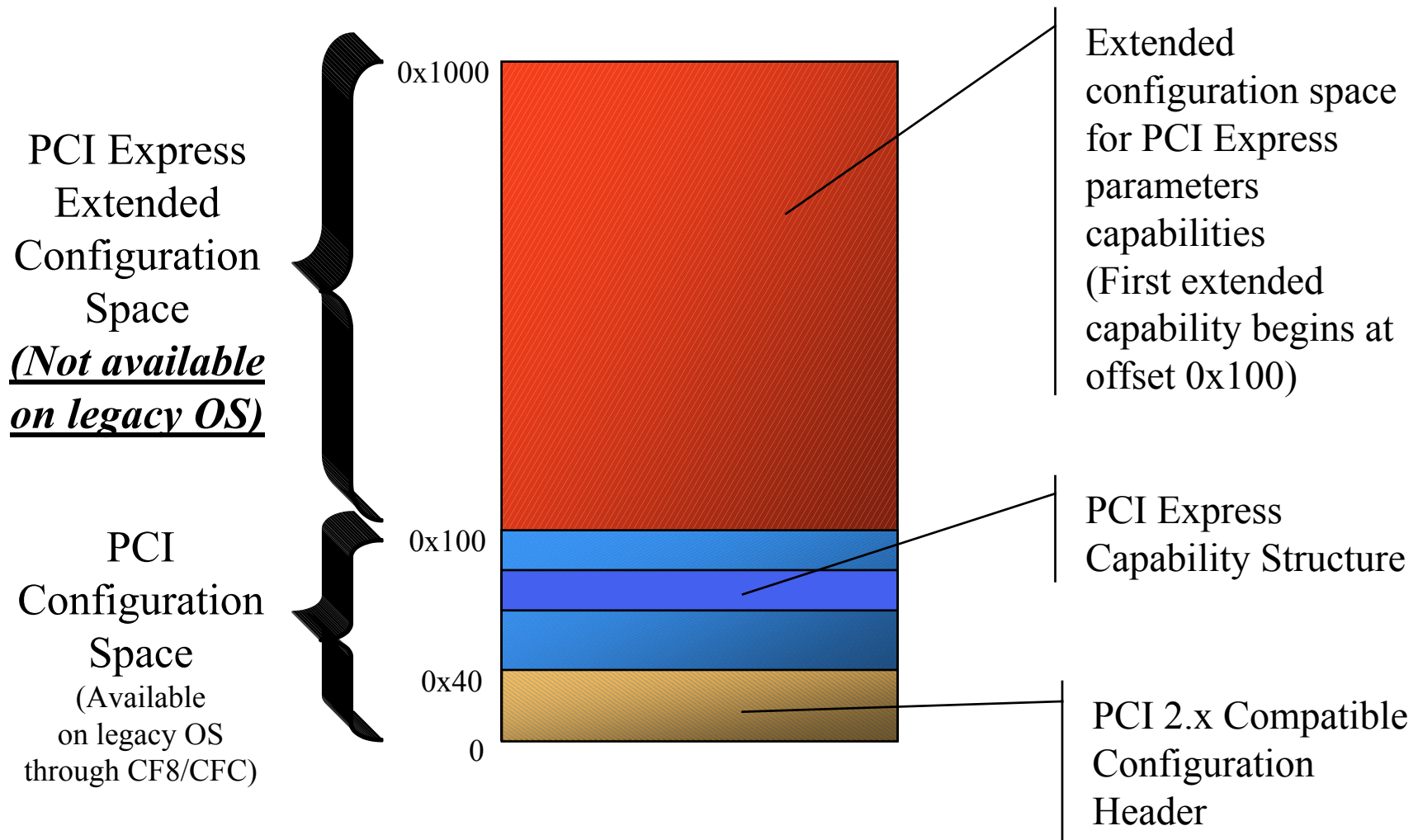
- In conventional PCI and PCI-X, we have
 - ✓ Devices
 - ✓ PCI-PCI bridges
 - ✓ Host bridges
- In PCI Express, we have
 - ✓ Endpoints
 - ✓ Switches
 - ✓ And a Root complex
- New PCI Express entities represented in configuration space using existing PCI concepts and registers to maintain backward compatibility

Config Space Representation



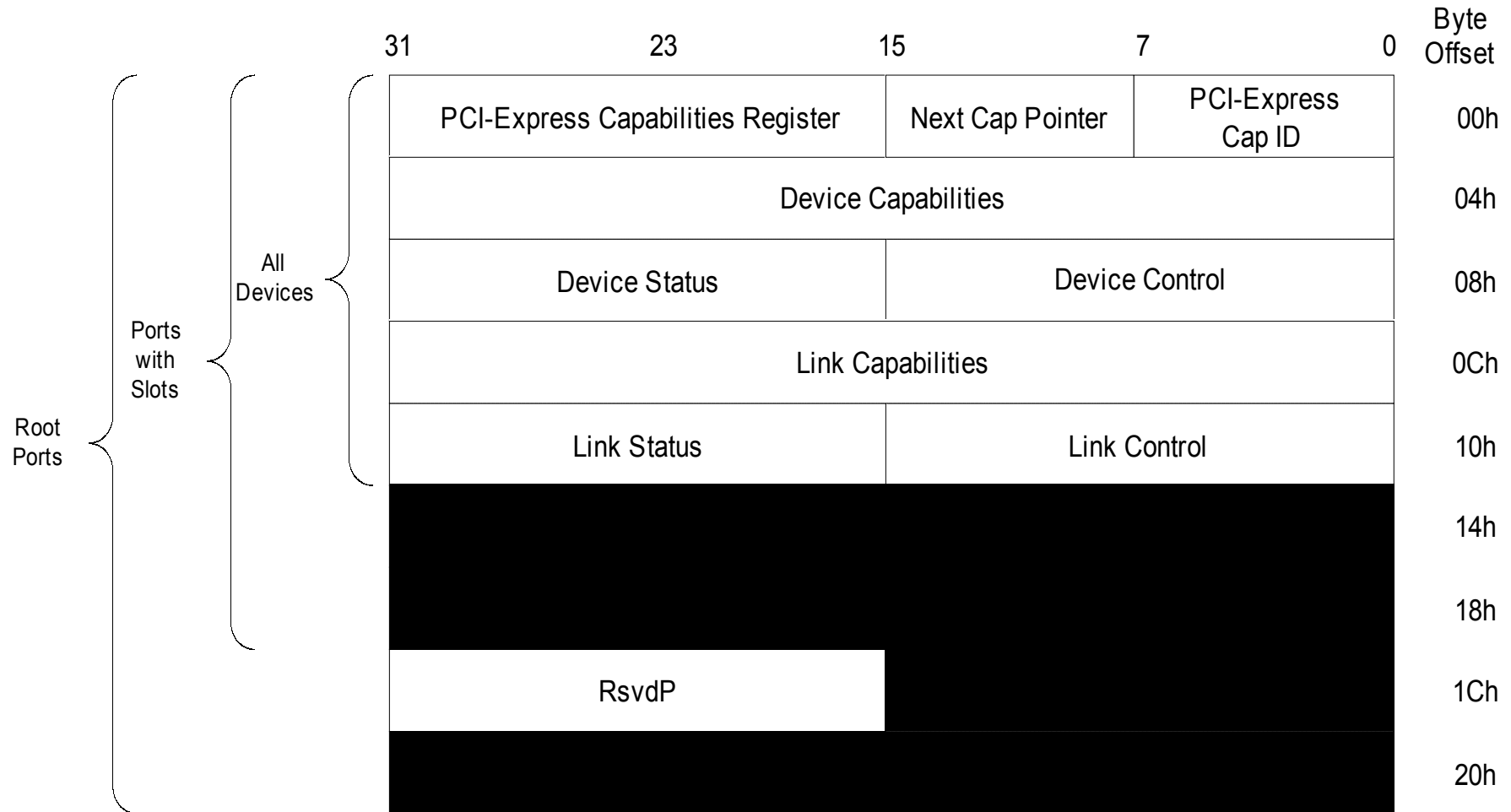


Configuration Space Layout



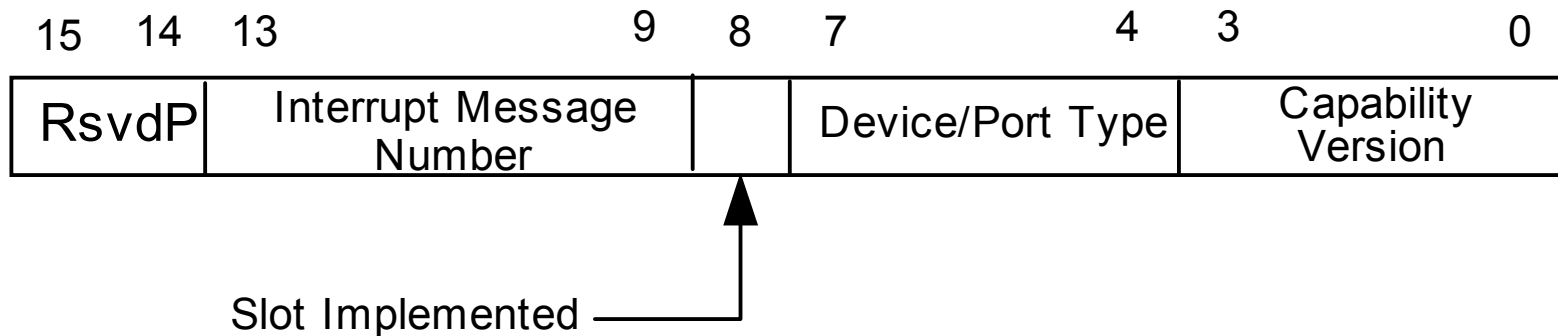


PCI Express Capability Structure





PCI Express Capability Structure Header

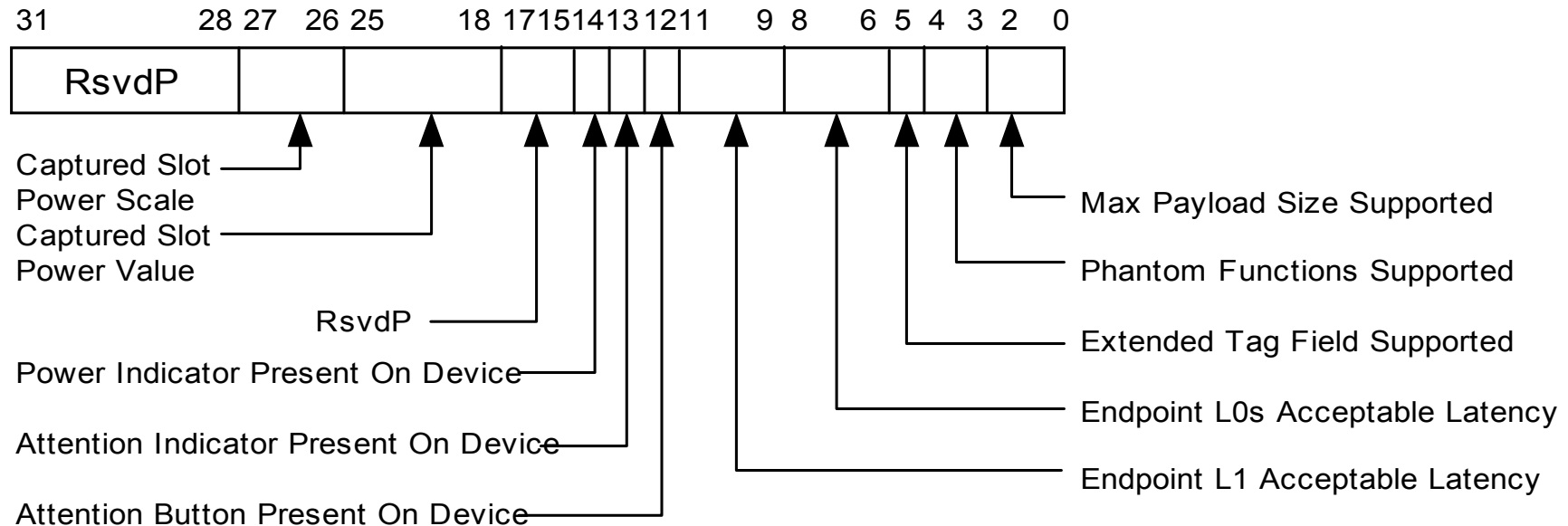


- **Slot Implemented and Interrupt Message Number fields are valid for Root Ports and Switch Downstream Ports**
- **Slot registers ignored if Slot Implemented bit is not set (e.g. motherboard down devices)**



PCI Express Capability Structure

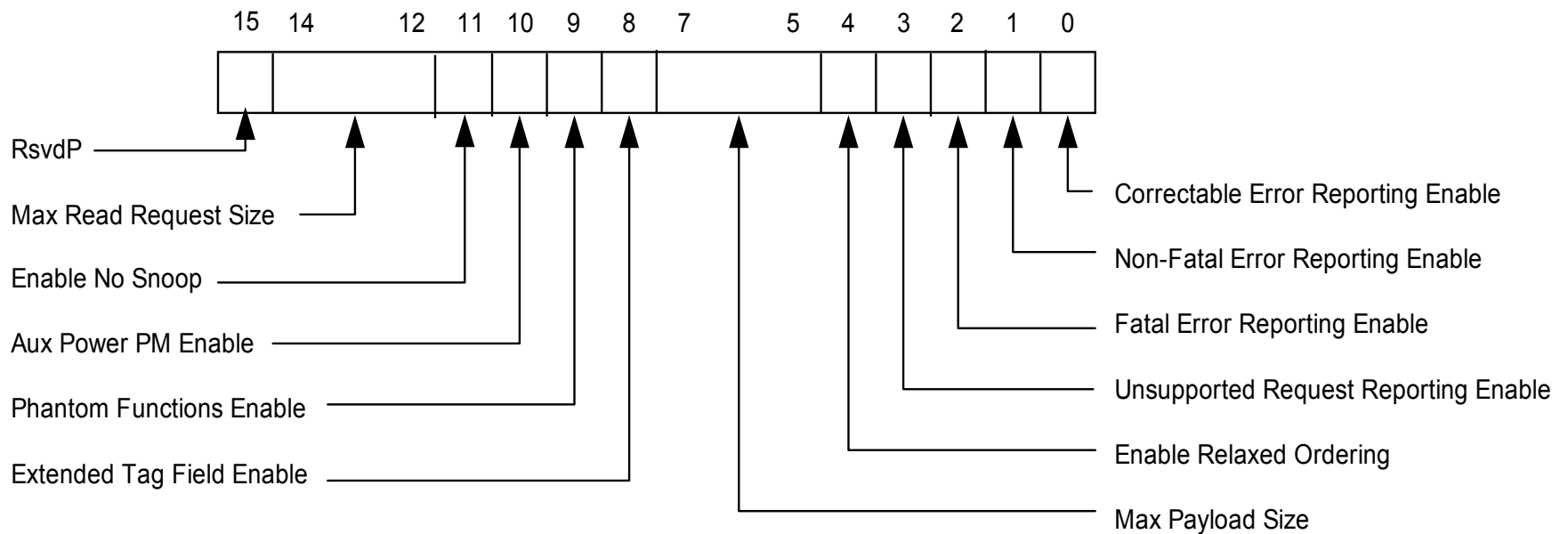
Device Capabilities



- **Endpoint acceptable latencies valid only for endpoint devices**
- **Slot power fields indicate power available at upstream link of component**

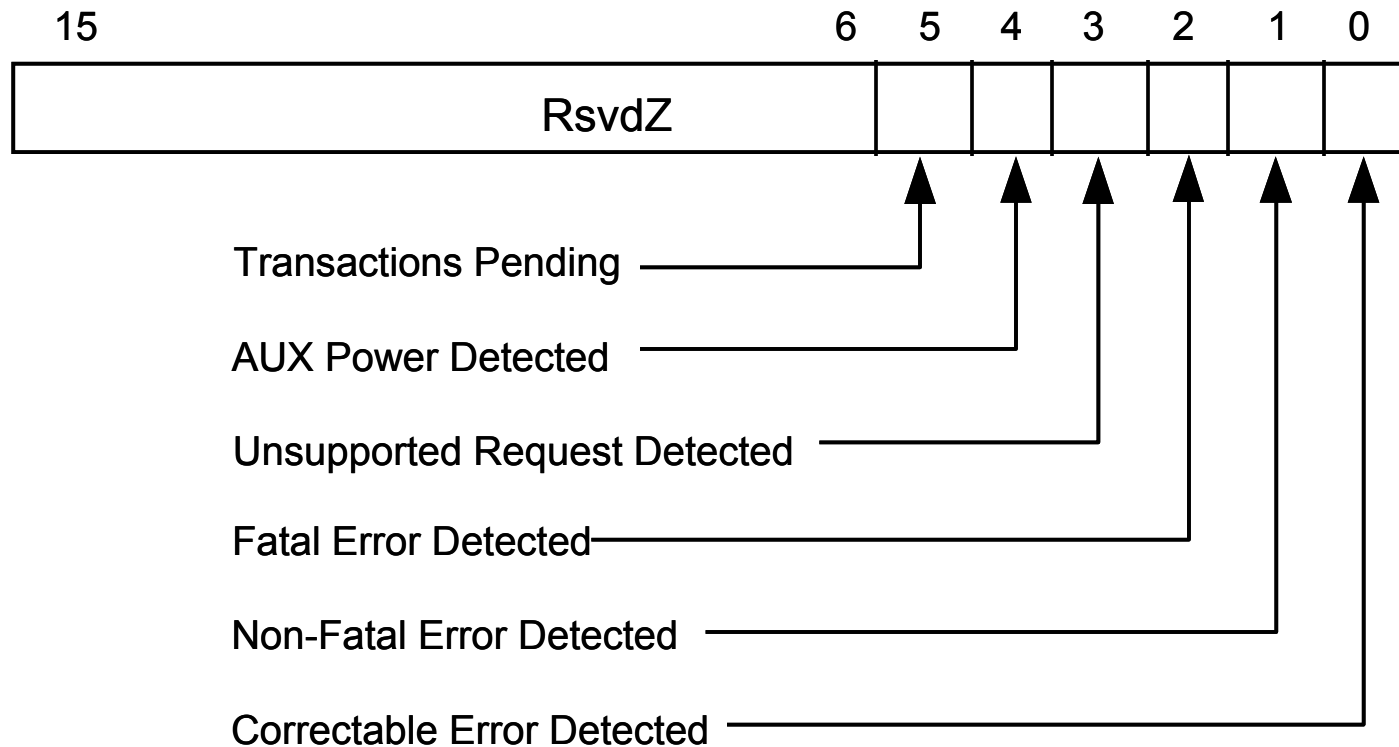


PCI Express Capability Structure Device Control





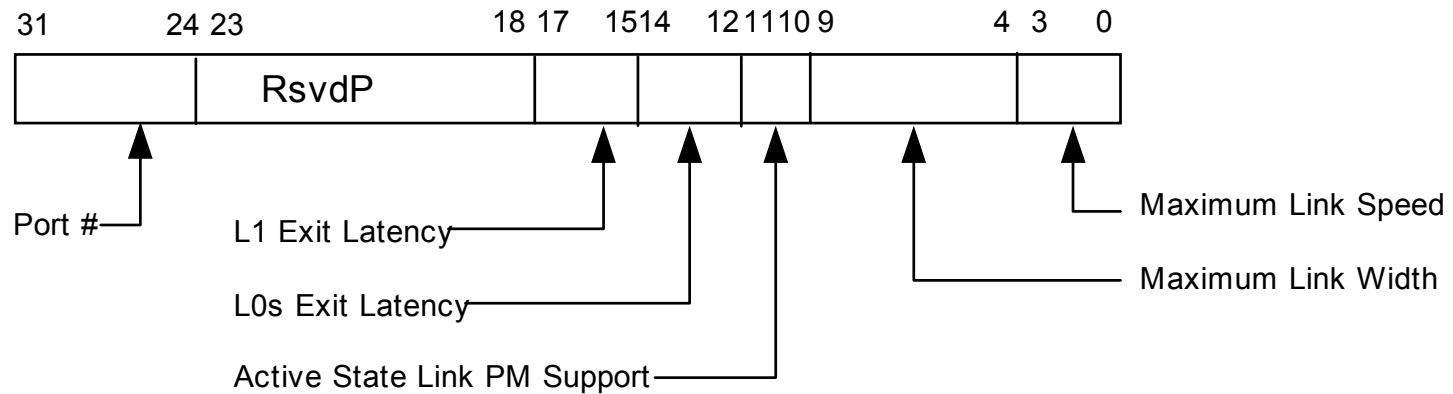
PCI Express Capability Structure Device Status





PCI Express Capability Structure

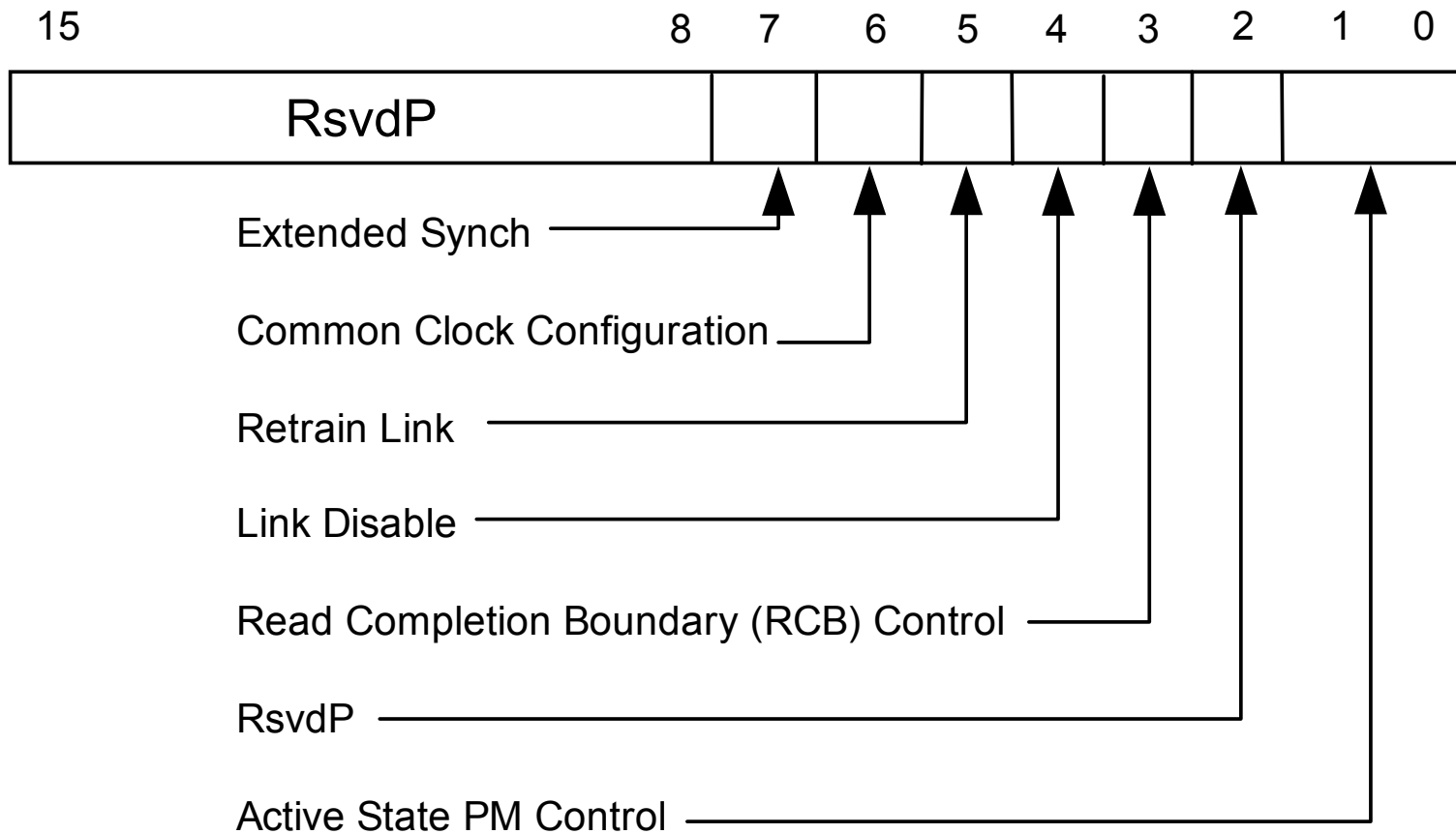
Link Capabilities





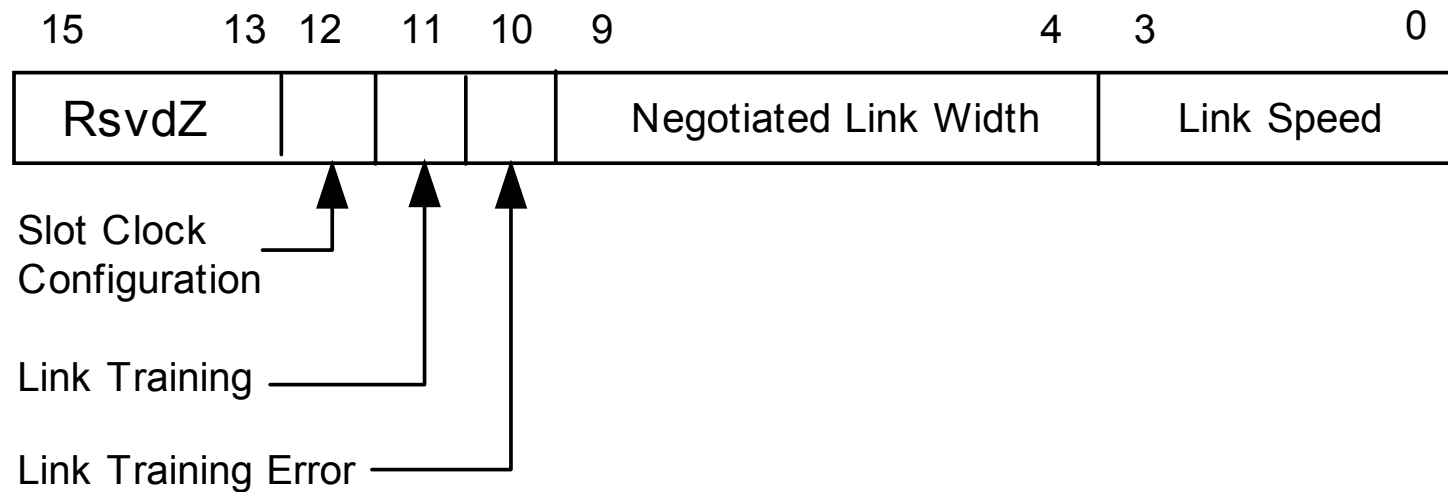
PCI Express Capability Structure

Link Control





PCI Express Capability Structure Link Status



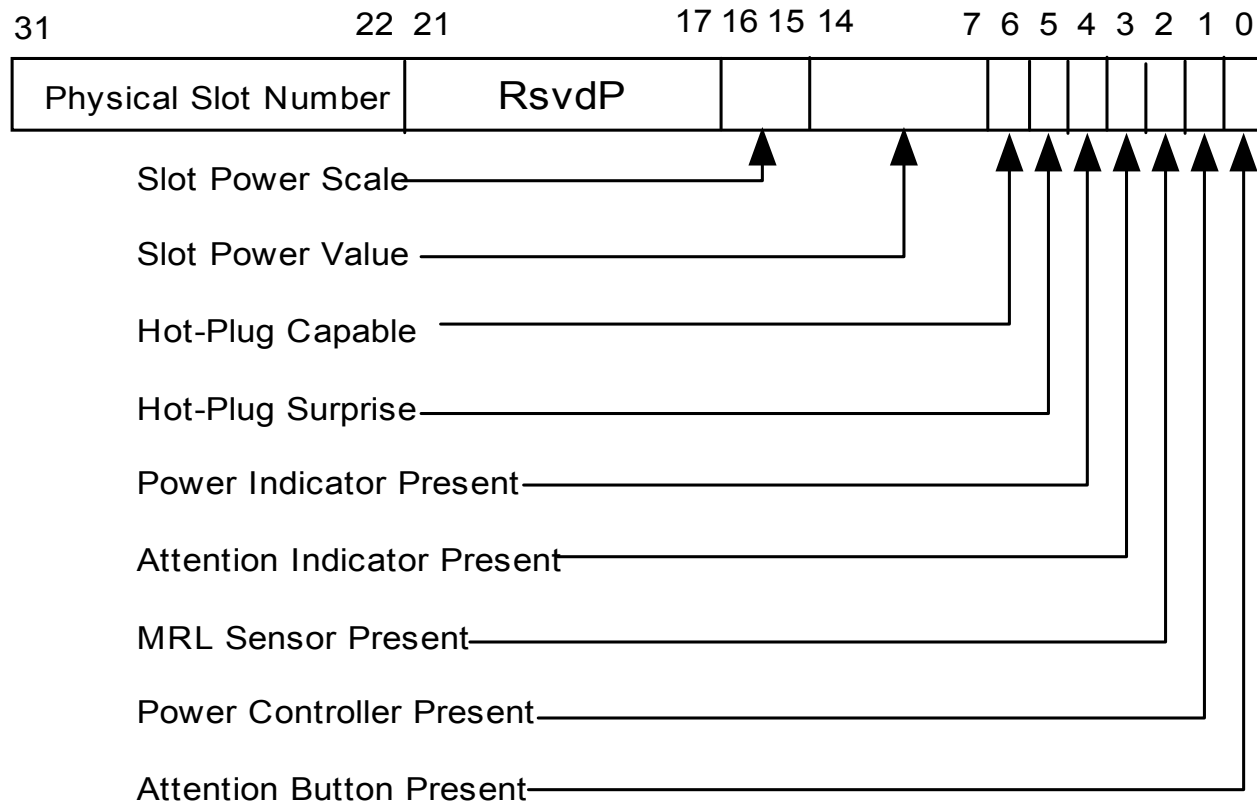


PCI Express Hot-plug Support

- PCI Express protocol and electricals designed from the ground up to support hot-plug
- Replaces SHPC as hot-plug mechanism for PCI Express
 - ✓ SHPC continues to be the mechanism for parallel bus PCI implementations.
- Flexibility in placing buttons/indicators by using PCI Express in-band messaging:
 - ✓ On the card (CompactPCI style)
 - ✓ On the chassis (SHPC style)
 - ✓ Not at all (PCCard style)
- Common usage model



PCI Express Capability Structure Slot Capabilities



➤ **Slot Power fields indicate power capabilities of slot**

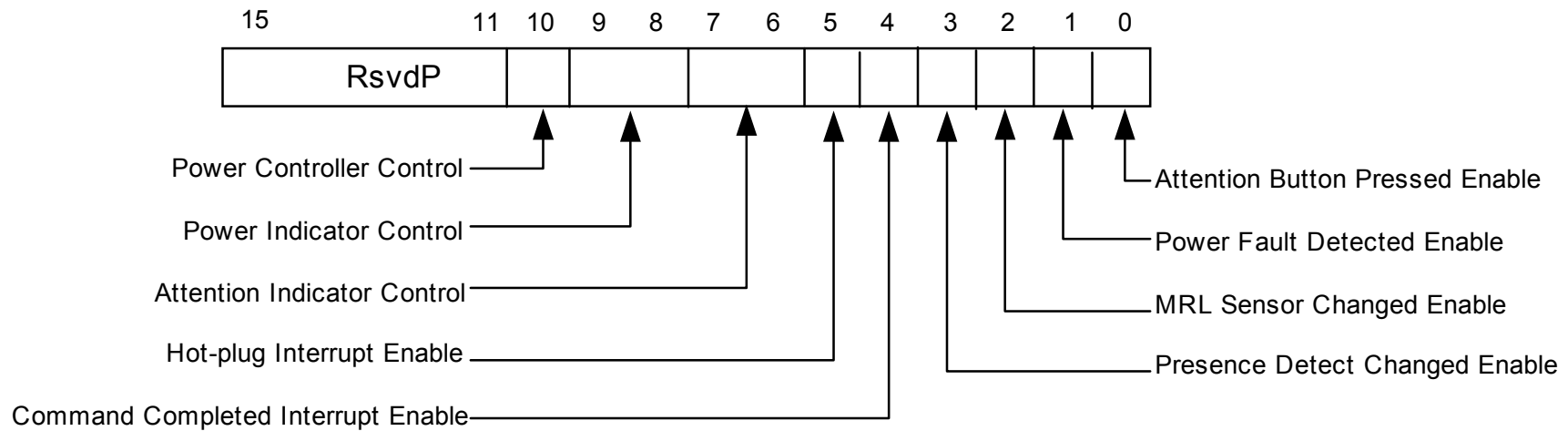


Native Hot-plug Support

- Simplified sensors and controllers that can be configured to support several different hot-plug models
 - ✓ Presence Detect Pins
 - ✓ Power & Attention Indicators
 - ✓ Power Controller (also detects Power Faults)
 - ✓ MRL Sensor
 - ✓ Attention Button
- Buttons/Indicators implemented either on card (device capabilities) or chassis (slot capabilities)
 - ✓ Slot to card communication using in-band messages

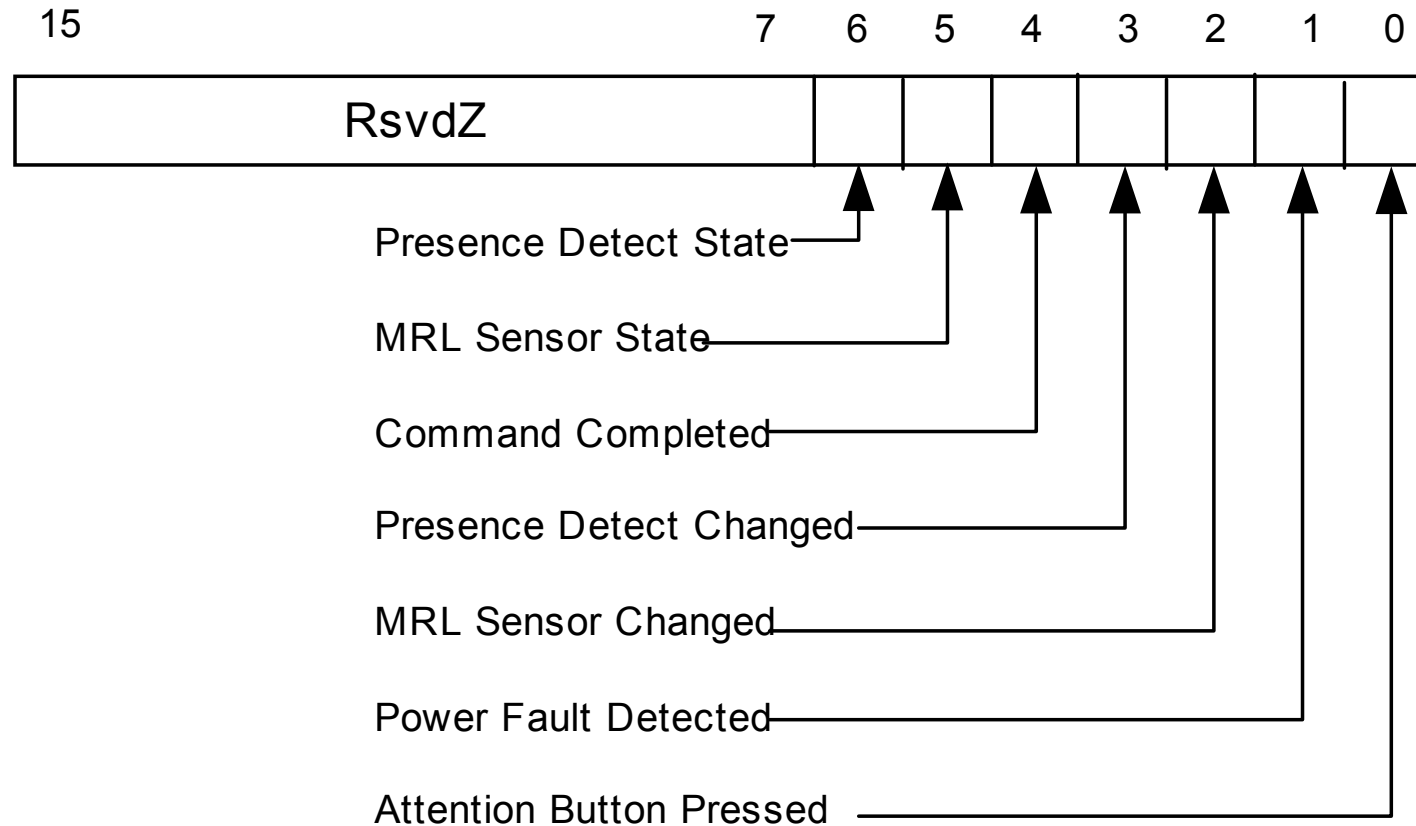


PCI Express Capability Structure Slot Control





PCI Express Capability Structure Slot Status



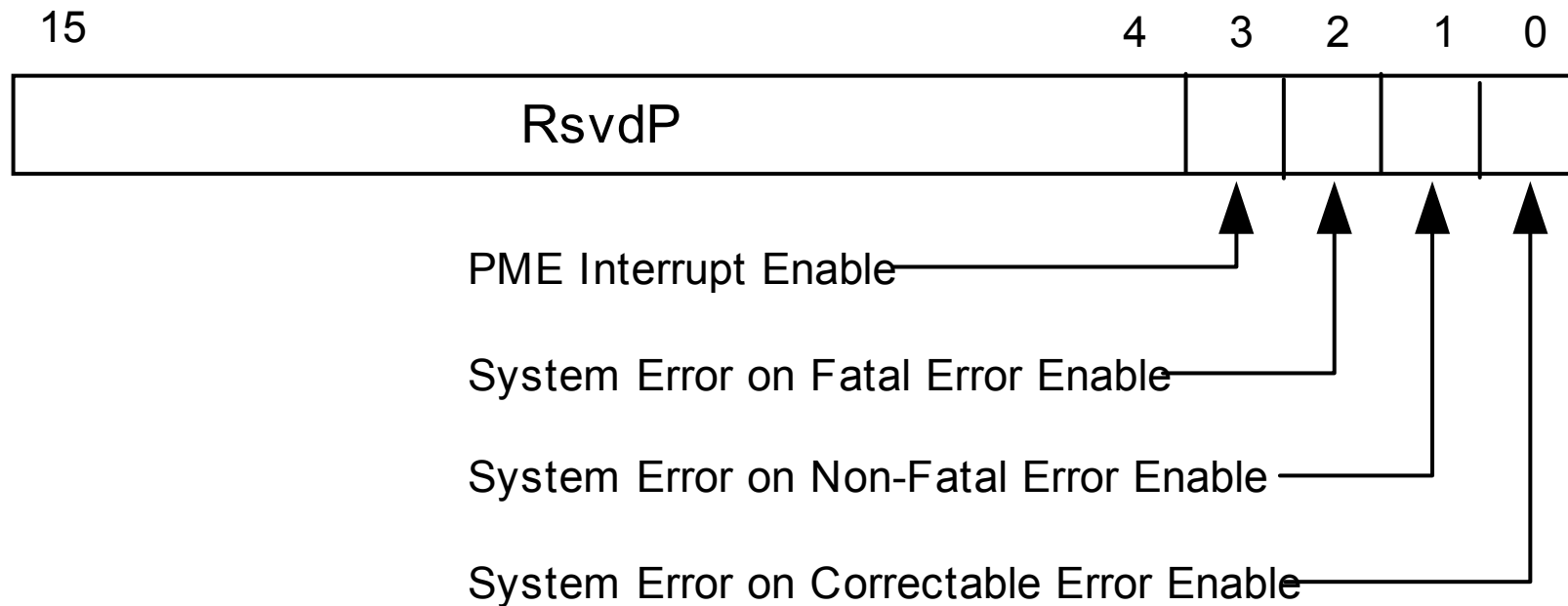


Root Port Capabilities

- Root port recipient of PME and error messages
- Root port registers allow software control of response to PME and error messages
- PME requestor ID latched by root port for identification of PME source

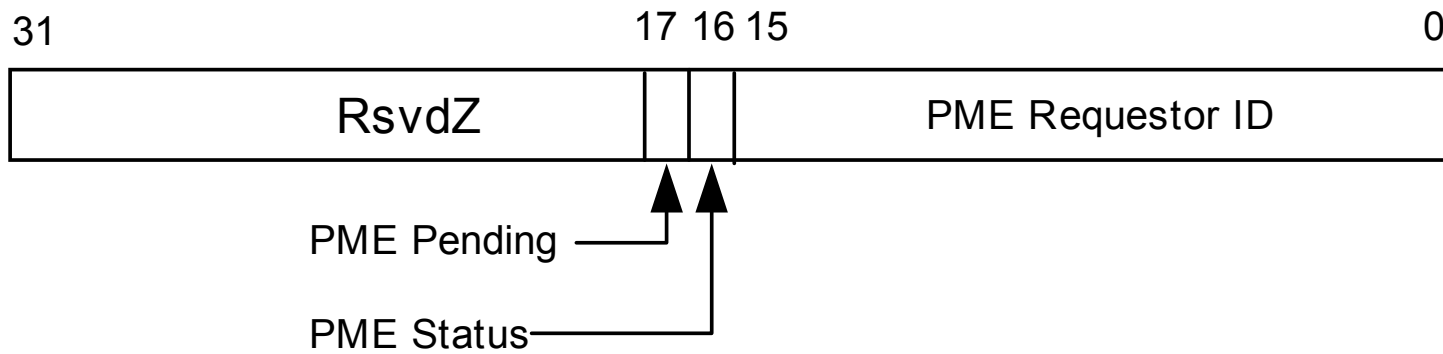


PCI Express Capability Structure Root Port Control





PCI Express Capability Structure Root Port Status





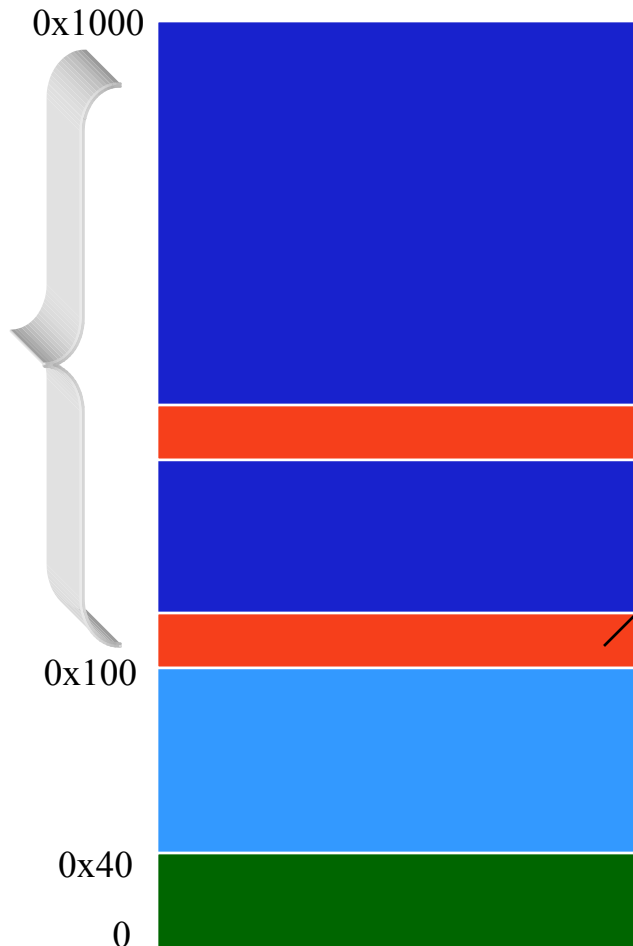
Extended Configuration Mechanism

- Extends device configuration space
- **Not accessible** on Legacy operating systems
- Flat memory mapped access for extended configuration
 - ✓ 4096 bytes of memory mapped space per device
 - ✓ First 256 bytes alias traditional PCI index/data configuration space
 - ✓ No index/data access
 - ✓ Located by base address + offset (bus, device, function)
 - ✓ Firmware communicates base address to OS



Extended Configuration Space Layout

Extended Configuration Space



PCI Express Extended Capability (Optional or Required)

PCI Express Capability ID	15:0 Capability ID 19:16 Capability Version Number 31:20 Next Capability Offset (0x0 based)
Capability Data	...
...	Length implied by CAP ID / Version Number

PCI Express extended capabilities start at base of extended configuration region

PCI Express enhances system configuration capability while preserving compatibility with PCI software.



Advanced Error Capability

- Base PCI Express has improved error reporting and control
- Optional advanced capabilities allow for:
 - ✓ Detection and logging of all correctable, uncorrectable and fatal errors
 - ✓ Support for collection of error data after a fatal reboot
 - Sticky bits
- Should help provide early warning for failing components



Advanced Error Capability

31	0	Byte Offset	
PCI-Express Enhanced Capability Header		00h	
Uncorrectable Error Status Register		04h	
Uncorrectable Error Mask Register		08h	
Uncorrectable Error Severity Register		0Ch	
Correctable Error Status Register		10h	
Correctable Error Mask Register		14h	
Advanced Error Capabilities and Control Register		18h	
Header Log Register		1Ch	
Only Valid for Root Ports	Root Error Command		2Ch
	Root Error Status		30h
	Error Source Identification Register	Correctable Error Source Identification Register	34h



Advanced Error Reporting

- Uncorrectable Errors
 - ✓ Mask, Status and Severity Controls
 - ✓ Severity controls Fatal or Non-Fatal
- Correctable Errors
 - ✓ Mask and Status Controls
- Error Pointer identifies First Uncorrectable Error
- Root Complex specific controls/status
 - ✓ Requestor ID for fault isolation
 - ✓ Interrupt generation for handling errors



Traffic Classes/Virtual Channels

- All PCI Express transactions are tagged as belonging to a traffic class (TC)
 - ✓ 8 possible Traffic Classes
 - ✓ All devices must support TC0, use of other TCs is optional
- Traffic Classes mapped to Virtual Channels for flow control/arbitration at ingress/egress ports
 - ✓ Each VC is an independently ordered stream
 - Multi-plane ordering model
 - PCI ordering rules only apply to transactions within the same VC
 - TC0-VC0 mapping required for PCI compatibility
 - ✓ Flexible VC/Port arbitration policies based upon priority, weighted round-robin (WRR) or time-based WRR schemes



QoS and Isochrony Mechanisms

- Switches can be configured to provide varying priorities to each TC and thus provide QoS.
 - ✓ Could be used on network card to support 802.1p QoS
- Switches can also be configured to provide bandwidth and latency guarantees for isochronous data.
 - ✓ Could be used in USB or 1394 controller
 - ✓ Glitch free audio



Call to Action

- Prepare for PCI Express in your existing designs
 - ✓ Avoid I/O resources; use Memory Mapped IO
 - ✓ Implement MSI; make drivers robust for edge-triggered interrupt handling
- Take advantage of new PCI Express features, its not just fast serial PCI!
 - ✓ Native Hot-Plug and new Form Factors
 - ✓ QoS & Isoch
 - ✓ Advanced Error Reporting