



## PCI-SIG ENGINEERING CHANGE NOTICE

<b>TITLE:</b>	MSI-X ECN for PCI-X PT 2.0a
<b>DATE:</b>	November 24, 2003
<b>AFFECTED DOCUMENT:</b>	PCI-X Protocol Addendum to the PCI Local Bus Specification Revision 2.0a
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### **Part I**

#### **1. Summary of the Functional Changes**

Enhance PCI-X to support MSI-X, as defined in the MSI-X ECN for PCI 2.3. Require PCI-X devices that support interrupts to implement MSI or MSI-X or both.

#### **2. Benefits as a Result of the Changes**

PCI-X systems can take advantage of the benefits offered by MSI-X over MSI, notably:

1. Supports a larger maximum number of vectors (2048 instead of 32).
2. Supports independent message address and message data for each vector.
3. Supports per-vector masking; adds per-vector masking as a new optional feature for MSI.
4. Enables more flexibility when software allocates fewer vectors than hardware requests.

#### **3. Assessment of the Impact**

Subsequent pages detail the changes required for the PCI-X PT specification.

#### **4. Analysis of the Hardware Implications**

PCI-X devices that support interrupts are now permitted to implement MSI-X in addition to MSI, or in lieu of MSI.

#### **5. Analysis of the Software Implications**

1. If a device implements MSI-X in addition to MSI, any existing software that supports only MSI will not recognize the MSI-X capability, and will operate using MSI. New software that supports MSI-X can take advantage of MSI-X's benefits over MSI.
2. If a device implements MSI-X in lieu of MSI, any existing software that supports only MSI will not recognize the MSI-X capability, and will be unable to configure the device to use messages to signal interrupts. It is believed that little if any such software exists.

## Part II

### Detailed Description of the change

*Terms and Acronyms, p. 32, add the following entry:*

#### Message Signaled

Interrupt (MSI/MSI-X) Two similar but separate mechanisms that enable a device to request service by writing a system-specified DWORD of data to a system-specified address using a memory write transaction. MSI is defined in PCI 2.3. MSI-X is a separate extension mechanism defined in the MSI-X ECN for PCI 2.3. Compared to MSI, MSI-X supports a larger maximum number of vectors and independent message address and data for each vector.

*2.5. Attributes, p. 73, change text as shown:*

**Table 2-9: Burst and DWORD Requester Attribute Field Definitions**

Attribute	Function
...	...
No Snoop (NS)	... <del>This attribute is used only for memory transactions that are not Message Signaled Interrupts (as defined in PCI 2.3).</del> The requester must not set this bit if the transaction is <del>a Message Signaled Interrupt</del> an MSI, MSI-X, I/O, Special Cycle, or Device ID Message transaction. (See Section 2.7.2.2 for configuration transactions and Section 2.10.4 for Split Completions.) ...
Relaxed Ordering (RO)	... <del>This attribute is used only for memory transactions that are not Message Signaled Interrupts (as defined in PCI 2.3), and for device ID messages.</del> The requester must not set this bit if the transaction is <del>a Message Signaled Interrupt</del> an MSI, MSI-X, I/O, or Special Cycle transaction. (See Section 2.7.2.2 for configuration transactions, Section 2.10.4 for Split Completions, and Section 2.16.2 for device ID messages.) ...

3.2. *Message-Signaled Interrupts*, p. 198, change text as shown:

## **3.2 Message-Signaled Interrupts (MSI/MSI-X)**

Support of message-signaled interrupts is optional for systems and system software.

PCI-X devices that generate interrupts are required to support [MSI or MSI-X or both](#). ~~message-signaled interrupts and must support a 64-bit message address. If MSI is supported, the device must implement the 64-bit Message Address version of the MSI capability structure. Implementation of these features is specified in PCI 2.3.~~ Devices that require interrupts in systems that do not support message-signaled interrupts must also implement interrupt pins.

System software must not assume that a message-capable device has an interrupt pin. Devices that rely on polling for device service in systems that do not support message-signaled interrupts are permitted to implement messages to increase performance in systems that do support it.

The requester of a message-signaled interrupt transaction must clear the No Snoop and Relaxed Ordering bits in the Requester Attributes.