

**Errata for the PCI-X Electrical and Mechanical
Addendum, Revision 2.0a**

Rev B.5

12/10/03

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Content Errata

This section corrects errors that affect the technical meaning of the specification and clarifies ambiguous or incomplete areas of the specification. These corrections will be included in a future revision of the specification.

C1. C/BE[4]# (FSTROBE[2]) and C/BE[5]# (SSTROBE[2]) Swapping with AD[49::48]

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The present description of the way C/BE[4]# (FSTROBE[2]) and C/BE[5]# (SSTROBE[2]) swap with AD[49::48] when switching between Mode 1 and Mode 2 does not clearly explain that this swapping occurs inside the devices connected to the bus. Furthermore, it is not clear that Mode 2 data strobe grouping for length matching and group separation applies to the Mode 2 function of these pins.

Change Section 2.2.3, page 78, as follows:

For PCI-X Mode 2 add-in cards, the electrical length of each Category 1 signal within a source-synchronous signaling group (as defined in Table 2-11) must be matched to its associated data strobes. For signals that swap locations between Mode 1 and Mode 2 (as described in Section 2.6.2), these length-matching requirements apply only to the Mode 2 locations. Table 2-25 shows the maximum base difference that the add-in card is permitted to have between the signals and data strobes within a group. The base difference is the difference in length excluding differences for package electrical length compensation for the device (described below).

Package electrical length is measured from the device pin to the device pad. The vendor of a Mode 1 or Mode 2 device is permitted to specify an amount of electrical length that must be added to or subtracted from the add-in card base electrical length for each Category 1 signal within a group to compensate for differences in package electrical length. The vendor is permitted to specify a different amount of compensation for each signal within the group. Table 2-25 shows the maximum electrical length compensation that the device vendor is permitted to specify for each signal within each group. If the device vendor does not specify any package compensation, the device meets all input and output specifications at the device pins.

Table 2-25: Add-in Card Signal Electrical Length Matching and Separation, Mode 2

Group Number (Note 1)	Maximum Base Difference Between Signals and Data Strobes	Maximum Device Package Compensation	Minimum Strobe-to-Strobe Separation (Note 2)	Units
0	±35	±75	±80	ps
1	±35	±75	±80	ps
2	±35	±75	±80	ps
3	±35	±75	±80	ps

Notes:

1. See Table 2-11 for source-synchronous signaling groups and their associated data strobes.

2. The electrical length on the add-in card of the data strobes of each source-synchronous signaling group must differ from the electrical lengths of the data strobes of all other groups by at least the minimum separation shown. This requirement applies to the base electrical length before any package electrical length compensation. Data signals within each group are recommended to be separated from the data signals of other groups by this same amount. Signal integrity is best when all signals in the groups are separated by the greatest amount possible. For signals that swap locations between Mode 1 and Mode 2 (as described in Section 2.6.2), these length-separation requirements apply only to the Mode 2 locations.

The electrical length on the add-in card of the data strobes for source-synchronous signaling groups must be separated by the minimums shown in Table 2-25. For data strobes assigned to pins that swap locations between Mode 1 and Mode 2 (as described in Section 2.6.2), these length-separation requirements apply only to the Mode 2 locations. (The system noise budget depends on the signals in different groups crossing the add-in card connector at different times to minimize the magnitude of the differential voltage on ground cause by signal return currents.)

Change Section 2.6.2, page 104, as follows:

2.6.2 Locations of FSTROBE[2], SSTROBE[2], and AD[49::48]

~~In all cases, the C/BE# signals share pins with the data strobe signals and the differences between the electrical lengths of the data strobes and that of the rest of the signals within each source-synchronous signaling group is limited as described in Section 2.2.3. In all cases except C/BE[4]# (FSTROBE[2]) and C/BE[5]# (SSTROBE[2]), the add-in card connector pins for the data strobes are physically close to the rest of the pins in that source-synchronous signaling group. To make FSTROBE[2] and SSTROBE[2] pins close to their source-synchronous signaling group, C/BE[4]# swaps locations with AD[49] and C/BE[5]# swaps locations with AD[48] when the bus initializes in PCI-X Mode 2 relative to their locations in PCI-X Mode 1 and conventional mode.~~

~~The differences between the electrical lengths of the data strobes and that of the rest of the signals within each source-synchronous signaling group is limited as described in Section 2.2.3. To optimize the locations of the signals in Group 2 at the add-in card connector, the logical definitions of two pairs of pins on the connector are swapped when the bus initializes in PCI-X Mode 2. Specifically, the pins assigned to AD[49] and AD[48] in Mode 1 and conventional PCI mode become C/BE[4]# (FSTROBE[2]) and C/BE[5]# (SSTROBE[2]), respectively, when the bus initializes in Mode 2. Conversely, the pins assigned to C/BE[4]# and C/BE[5]# in Mode 1 and conventional PCI mode become AD[49] and AD[48], respectively, when the bus initializes in Mode 2. Each device on the bus must internally swap the functions assigned to these pins based on whether the bus initializes in Mode 1 or Mode 2.~~

~~This functional swapping is illustrated at the add-in card connector in Table 2-42. If the bus initializes in Mode 1, the logical function that each device connects internally to its I/O pin that connects to pin 78B of the add-in card connector is AD[49] and the logical function that the device connects internally to its I/O pin that connects to pin 66B is C/BE[4]#.~~

However, if the bus initializes in Mode 2, each device swaps these logical assignments, so the logical function it connects to pin 66B is AD[49] and the logical function it connects to pin 78B is C/BE[4]# (FSTROBE[2]). The same functional swapping occurs between the pins assigned to C/BE[5]# (SSTROBE[2]) and AD[48].

In Section 2.7, change the note at the bottom of Table 2-43, page 108, as follows:

Notes:

1. C/BE[4]# swaps locations with AD[49] and C/BE[5]# swaps locations with AD[48] when the bus initializes in PCI-X Mode 2 relative to their locations in PCI-X Mode 1 and conventional mode. In the rows in this table, the logical functions of these pins are shown with the Mode 1 function followed by the Mode 2 function. Electrical length matching and strobe-to-strobe separation requirements described in Section 2.2.3 apply only to the Mode 2 locations.

C2. Ringback Amplitude and Pulse Width at the Pin

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Additional analysis indicates that the worst-case amplitude of the ringback at the input pin is worse than described in the Appendix D. However, the specification for the signal at the input pad is accurate. This change applies only to the expected signal waveform observed at the package pin. No device characteristics are affected.

Change Table D-3, page 155, as follows:

Table D-3: Expected Actual Input Signaling Conditions

Symbol	Parameter	Min	Max	Unit	Note
I/O Voltage Levels					
$V_{ih(AC-pin)}$	Input High Voltage, Switching, at the package pin	$V_{ref} + 0.200$	$V_{I/O} + 0.650$	V	
$V_{il(AC-pin)}$	Input Low Voltage, Switching, at the package pin	-0.650	$V_{ref} - 0.200$	V	
Rise and Fall Times					
$T_{ir(pin)}$	Input Rise Time at the package pin	65	730	ps	1
$T_{if(pin)}$	Input Fall Time at the package pin	65	730	ps	2
ΔT_{irf}	Input Rise and Fall Matching Deviation	-200	200	ps	3
$slew_{irf(pin)}$	Instantaneous Input Rise and Fall Slew Rate		5.0	V/ns	4
Input Ringback					
V_{ihr}	Input High Ringback Voltage	$V_{ref} + 0.100$		V	
V_{ilir}	Input Low Ringback Voltage		$V_{ref} - 0.100$	V	
T_{ihr}	Input High Ringback Pulse Width		200300	ps	5
T_{ilir}	Input Low Ringback Pulse Width		200300	ps	6

Editorial Errata

This section corrects typographical, grammatical, and minor wording errors that do not affect the technical meaning of the specification. These corrections will be included in the next printing of this revision of the specification.

E1. Section Cross References

Posting Date: 12/10/03

The following cross references are incorrect:

Page	Location	Correction
165	2 nd paragraph	“on the add-in card (as required in Section 2.2.22.2.3)”

E2. Typographical Errors.

Posting Date: 12/10/03

1. Page 165, Section D.2.4, second paragraph.

Skews on the system board guarantee that adjacent signal groups arrive at the connector at different times when the source bridge is driving the bus. Skews on the add-in card (as required in Section 2.2.2) guarantee that signals in adjacent signal groups arrive at the connector at different times when the device on the add-in card is driving the bus.

- 2.

E3. Formatting Errors.

Posting Date: 12/10/03

1. The section numbers in the .pdf file “bookmark” screen do not accurately reflect the actual section numbers in the following places:
Section C.5.1.1-C.5.5
Section D.1.5.1-D.1.5.3

E4. Minor Wording and Figure Errors.

Posting Date: 12/10/03

1. Figure 2-19, page 43, and Figure 2-23, page 45, include protocol errors inconsistent with the requirements of PCI-X PT 2.0a. Each figure shows a three-data-phase transaction, but FRAME# is shown deasserting after the third data phase, when in fact, FRAME# should be shown deasserting on the third data phase, as correctly shown in Figure 2-68 in PCI-X PT 2.0a.

Furthermore, Figures 2-19, 2-20, 2-21, 2-23, 2-24, 2-25 all show turn-around of the target control

signals on a different clock than the one typically shown in PCI-X PT 2.0a. This is strictly an issue of documentation convention, since the target control signals are floating for several clocks, and the precise timing of the turn-around is artificial.

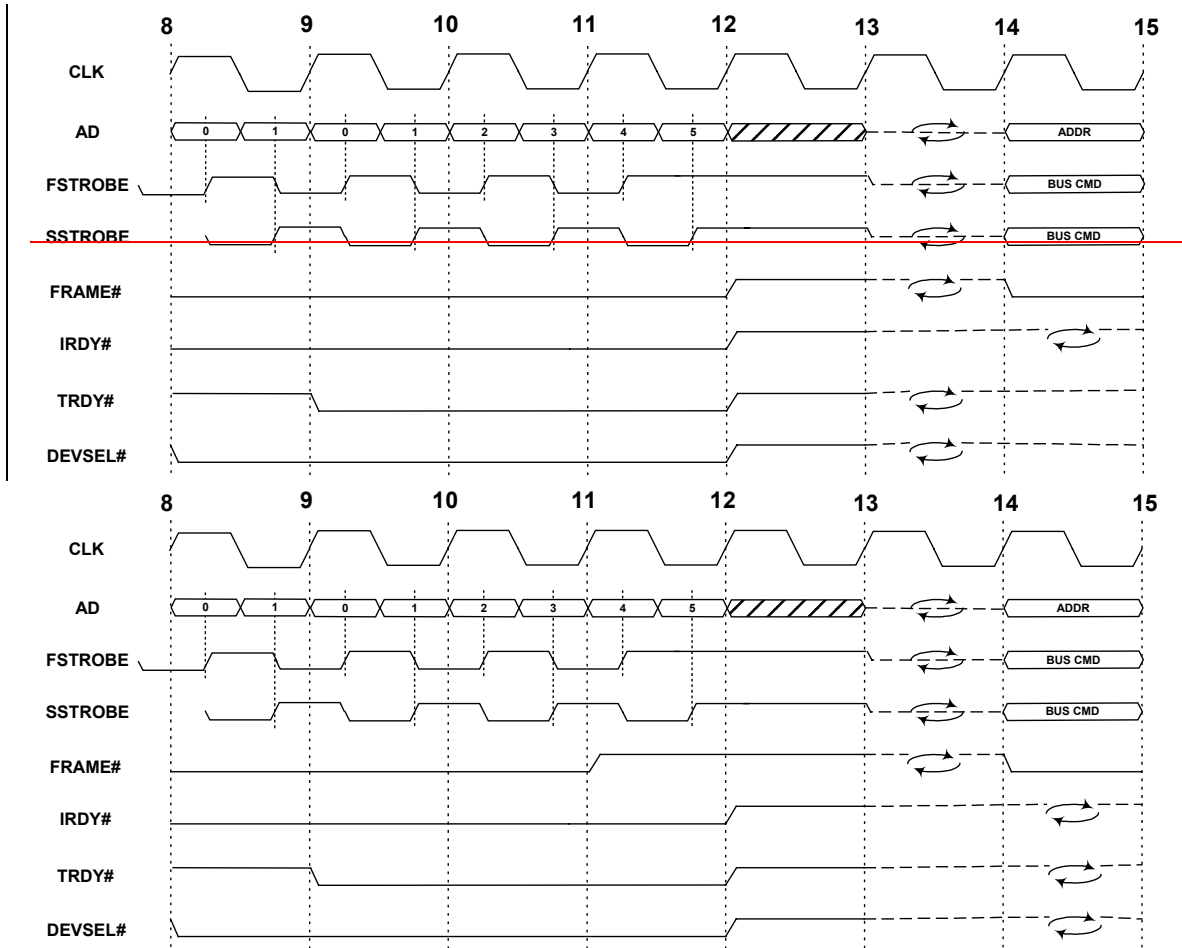


Figure 2-19: PCI-X 266 End of Data Strokes, Three Data Phases

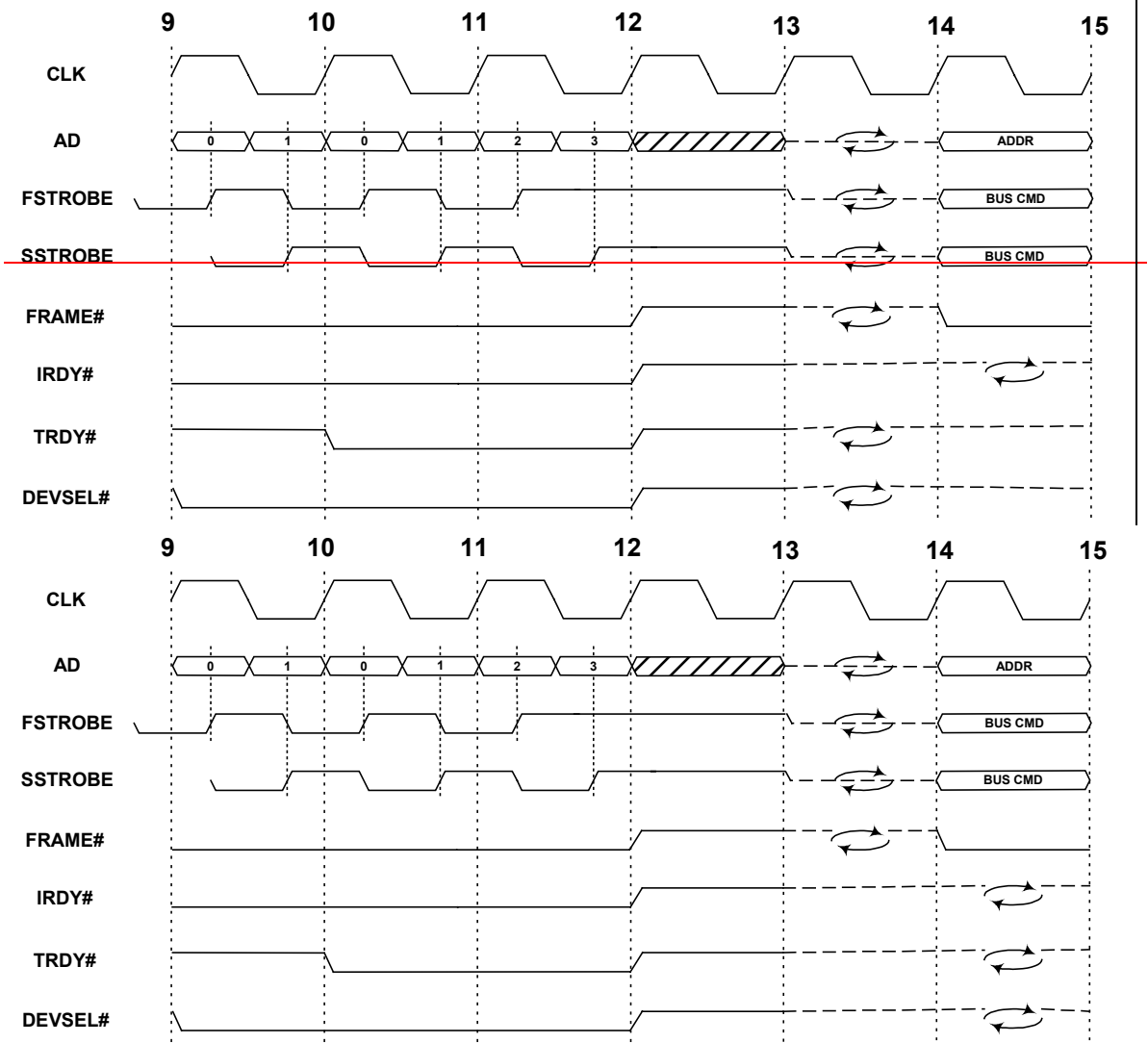


Figure 2-20: PCI-X 266 End of Data Strokes, Two Data Phases

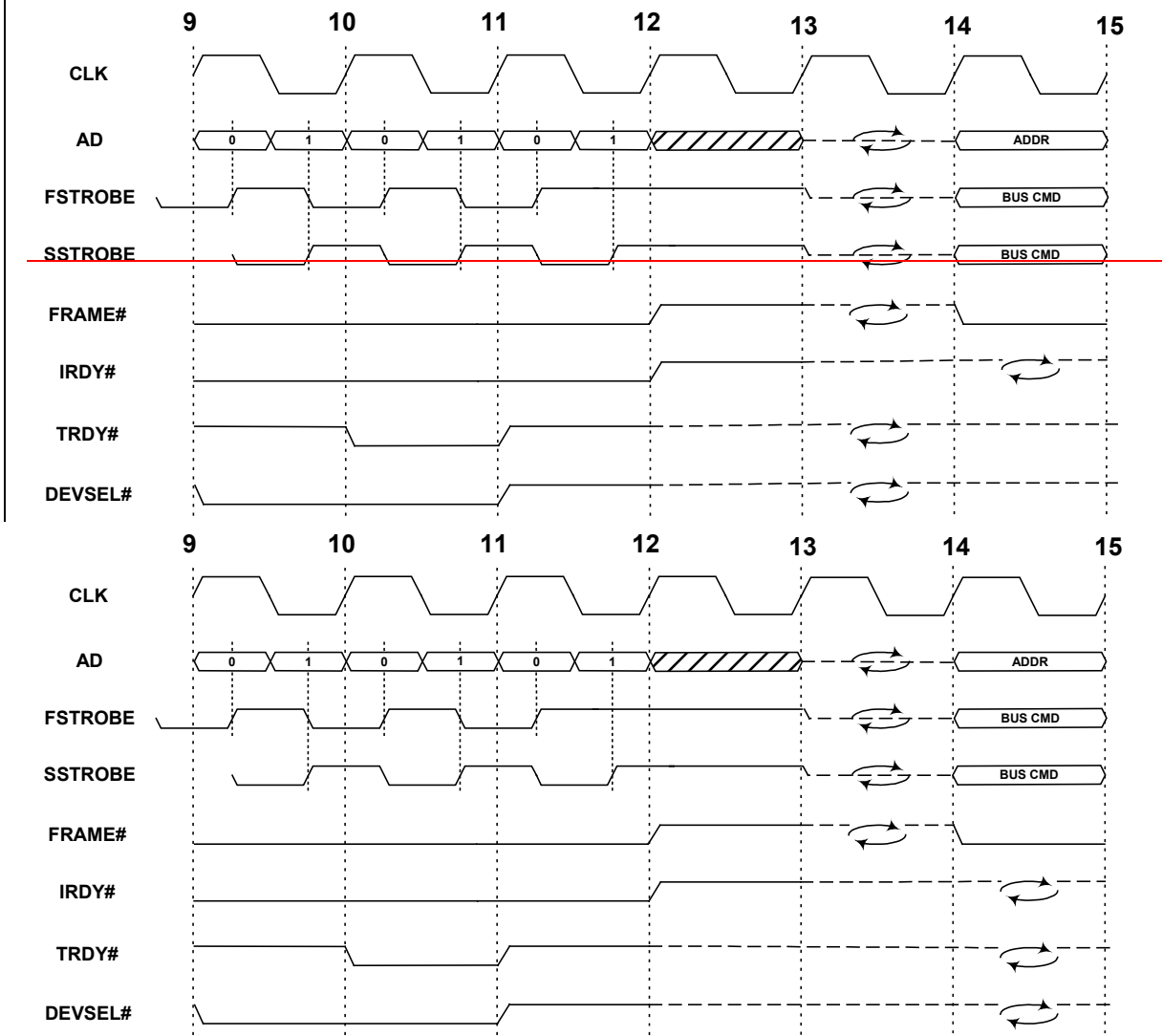


Figure 2-21: PCI-X 266 End of Data Strokes, One Data Phase

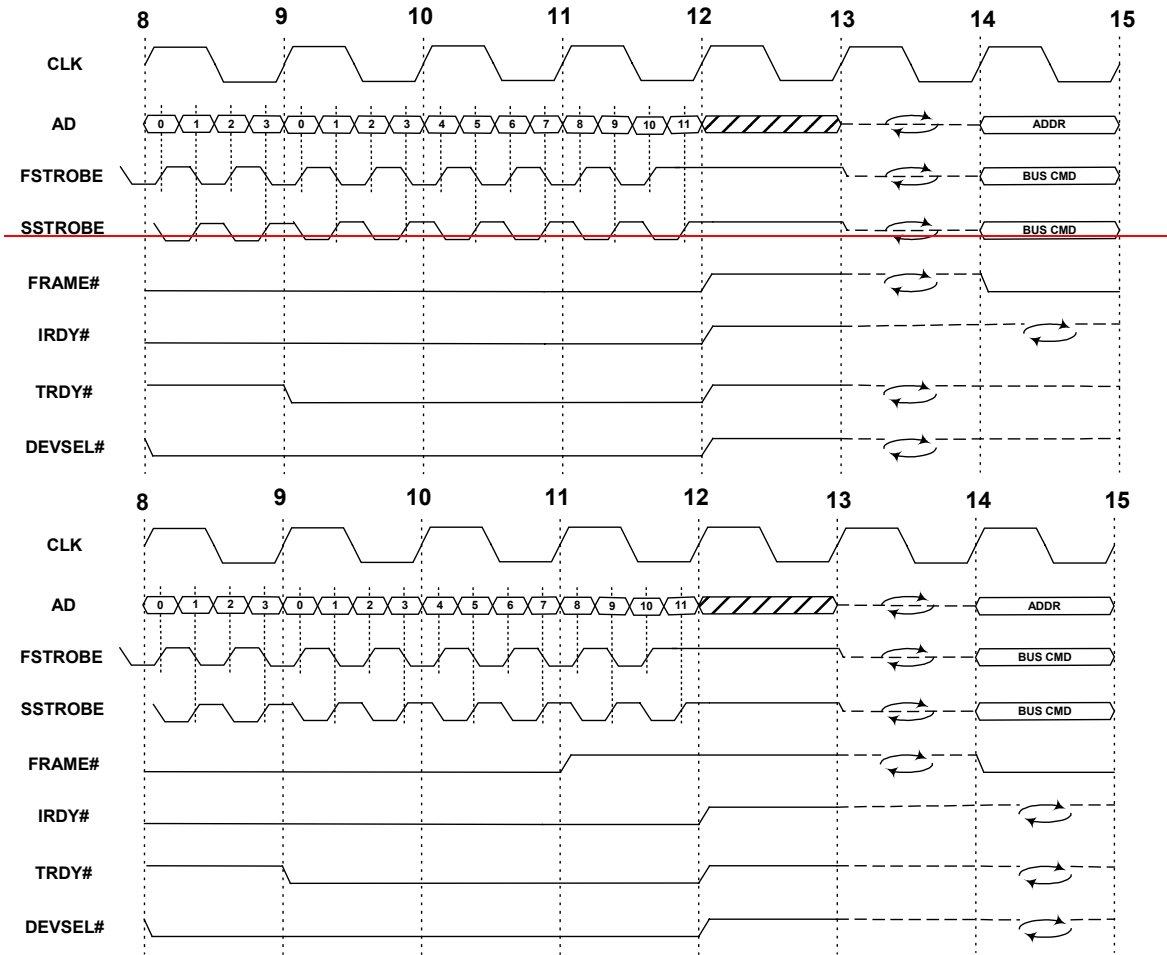


Figure 2-23: PCI-X 533 End of Data Strokes, Three Data Phases

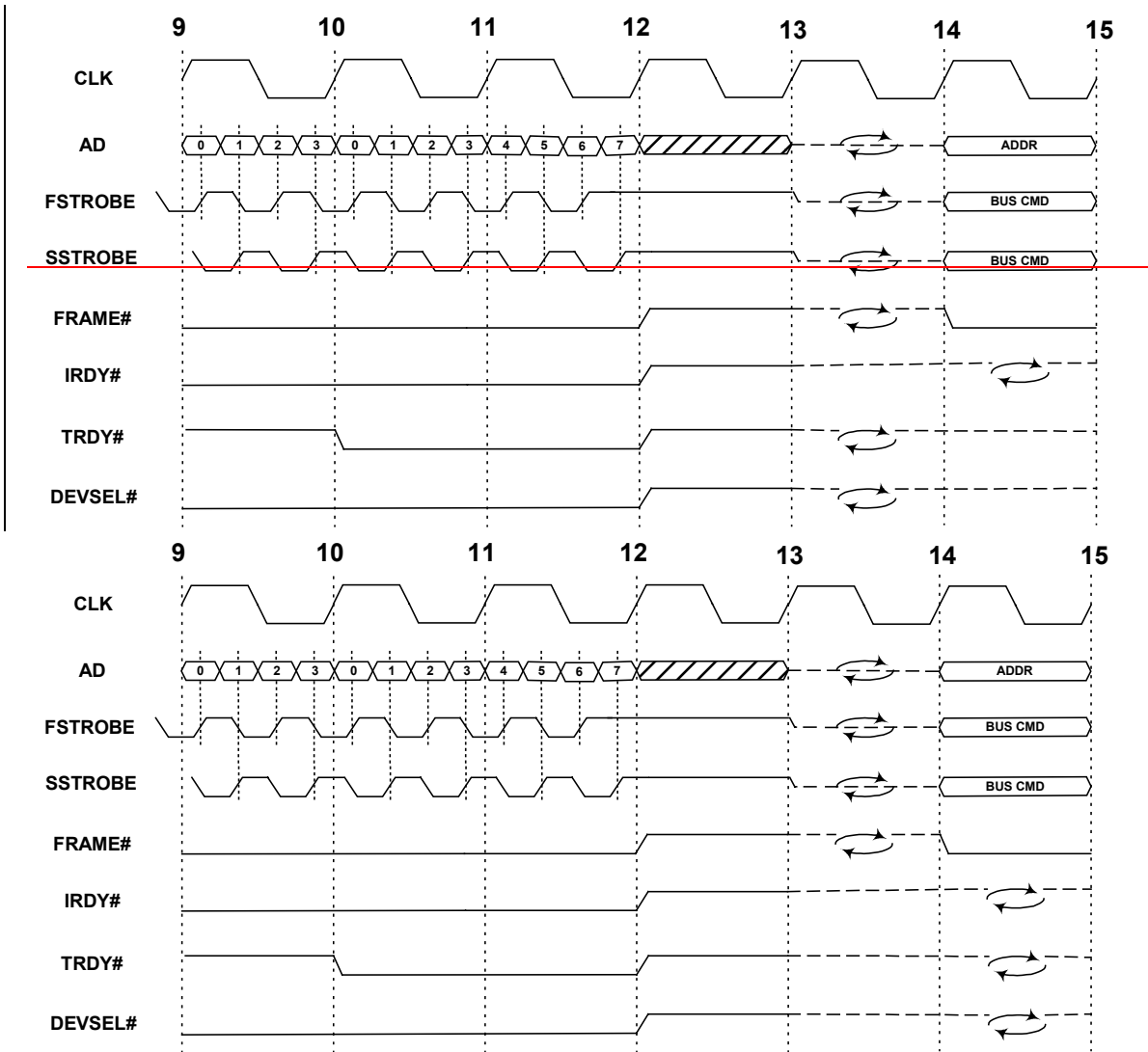


Figure 2-24: PCI-X 533 End of Data Strokes, Two Data Phases

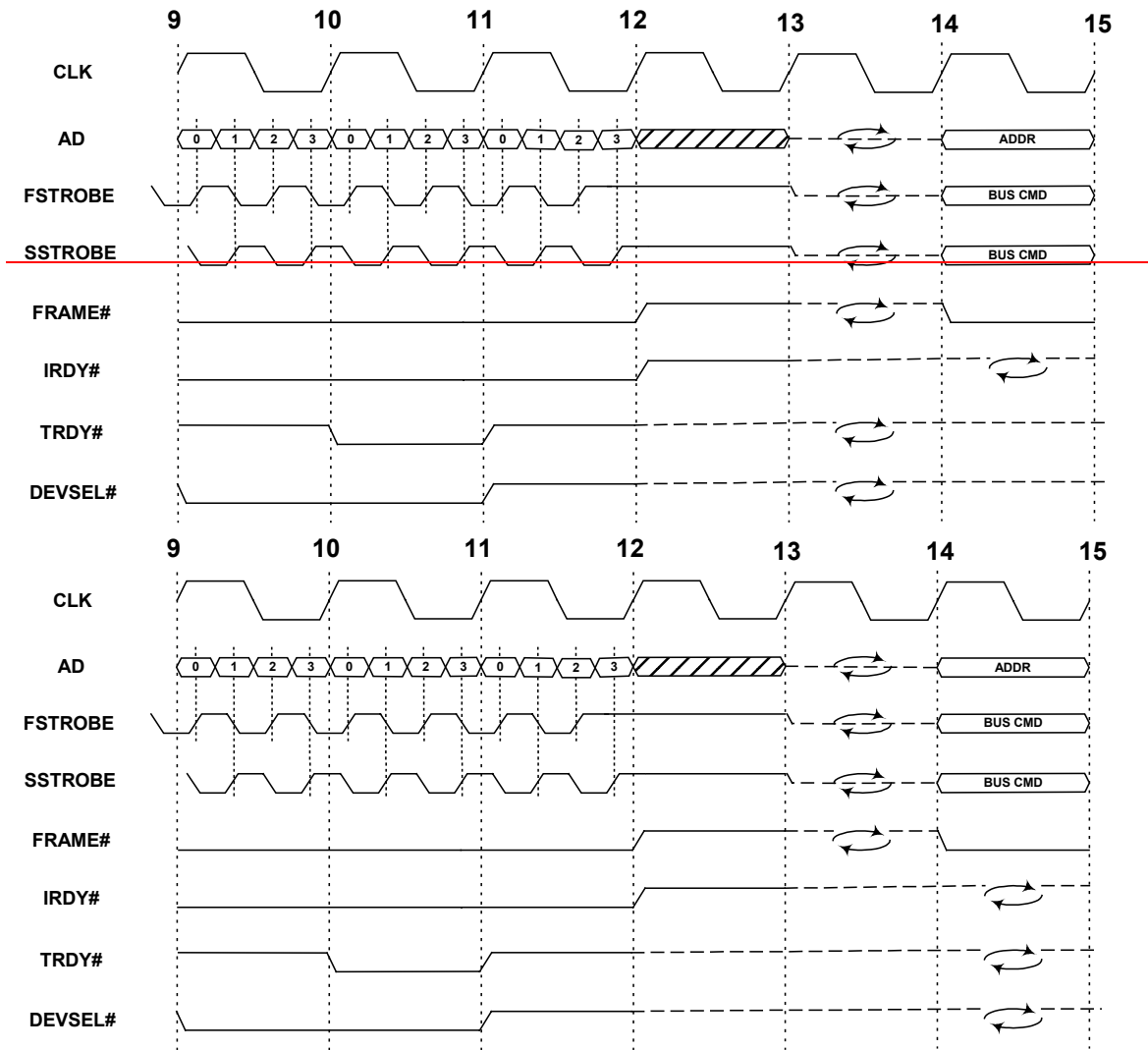


Figure 2-25: PCI-X 533 End of Data Strokes, One Data Phases

2. Section 2.3.6.2.1, page 91, change as follows:

Minimum signal propagation time for 3.3V signals operating in Mode 2 are measured ~~the~~ as described for Mode 1 in Section 2.3.6.1.

3. Section 2.1.2.4.2, page 32, Table 2-7, delete the phrase, “- based signals” from the definitions of T_{val} and T_{su} . This phrase was copied from PCI 2.3, but does not apply to PCI-X.

