

PCI



SIGTM

10TH YEAR ANNIVERSARY

PCI-X 2.0 Overview

PCI-X 2.0 Explained

What is PCI-X 2.0?



- **PCI-X 2.0 is a Faster Version of the Conventional PCI Standard**
 - ✓ PCI-X 2.0 uses the same PCI architecture
 - ✓ PCI-X 2.0 uses the same base protocols as PCI
 - ✓ PCI-X 2.0 uses the same BIOS as PCI
 - ✓ PCI-X 2.0 uses the same connector as PCI.
 - ✓ PCI-X 2.0 and PCI products are interoperable
 - ✓ PCI-X 2.0 uses the same driver models as PCI
- **However, PCI-X 2.0 is faster**
 - ✓ PCI-X 2.0 (PCI-X 533) is 32 times faster than the original version of PCI



- **Revision 2.0 of the Specification Introduces 2 New Speed Grades**

- ✓ **PCI-X 266**

- Uses Double Data Rate Technology to Achieve Data Rates of 266MHz
- Offers 2.13 Gigabytes per second of bandwidth
- Backward Compatible to All Speed Grades of PCI and PCI-X

- ✓ **PCI-X 533**

- Uses Quad Data Rate Technology to Achieve Data Rates of 533MHz
- Offers 4.26 GB/s Gigabytes per second of bandwidth
- Backward Compatible to All Speed Grades of PCI and PCI-X

PCI-X 2.0 Naming



- **PCI-X 1.0 Official Names**

- ✓ PCI-X 66
- ✓ PCI-X 133

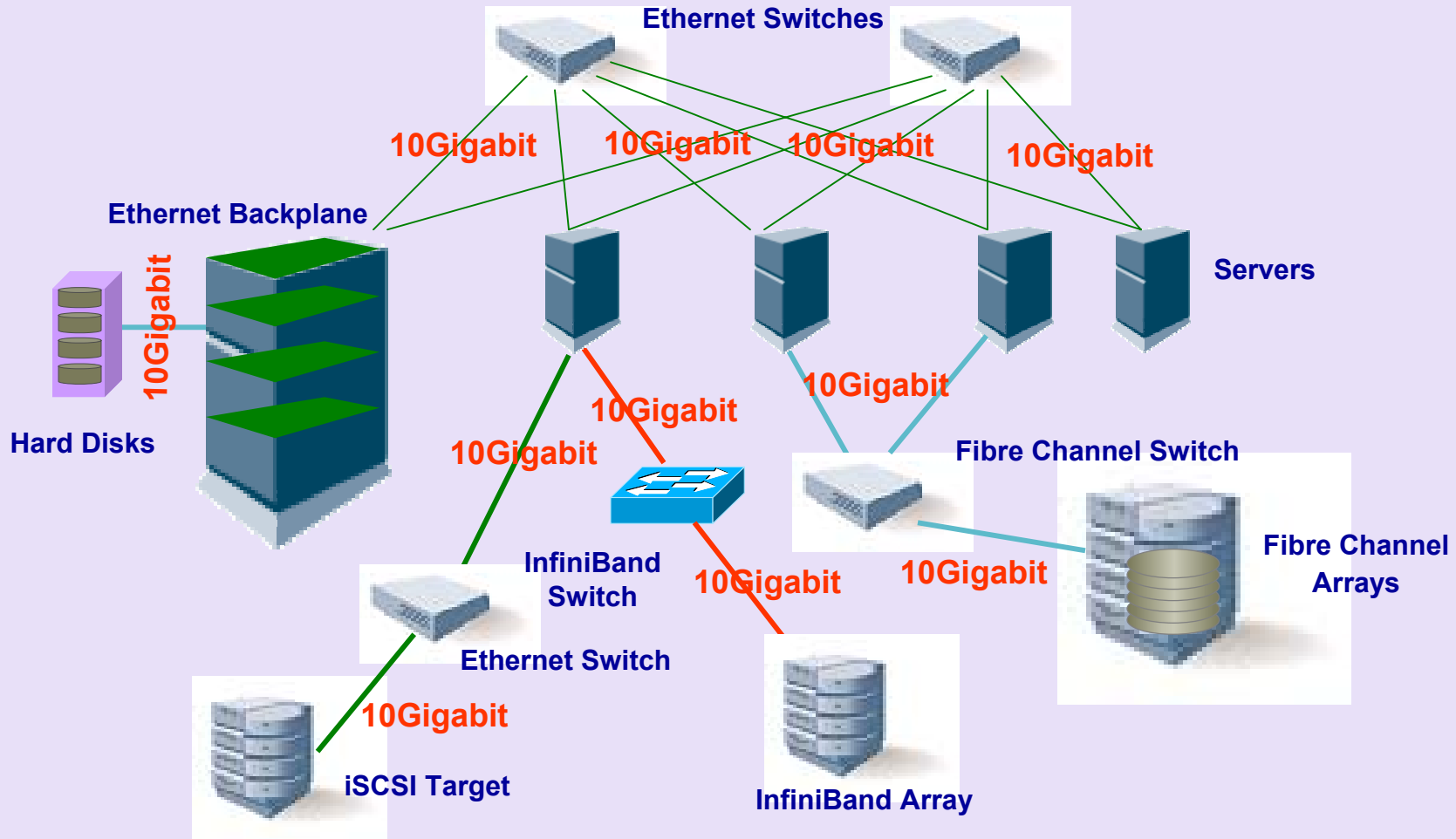
PCI-X 1.0 had 2 speed grades

- **PCI-X 2.0 Official Names**

- ✓ PCI-X 66
- ✓ PCI-X 133
- ✓ PCI-X 266
- ✓ PCI-X 533

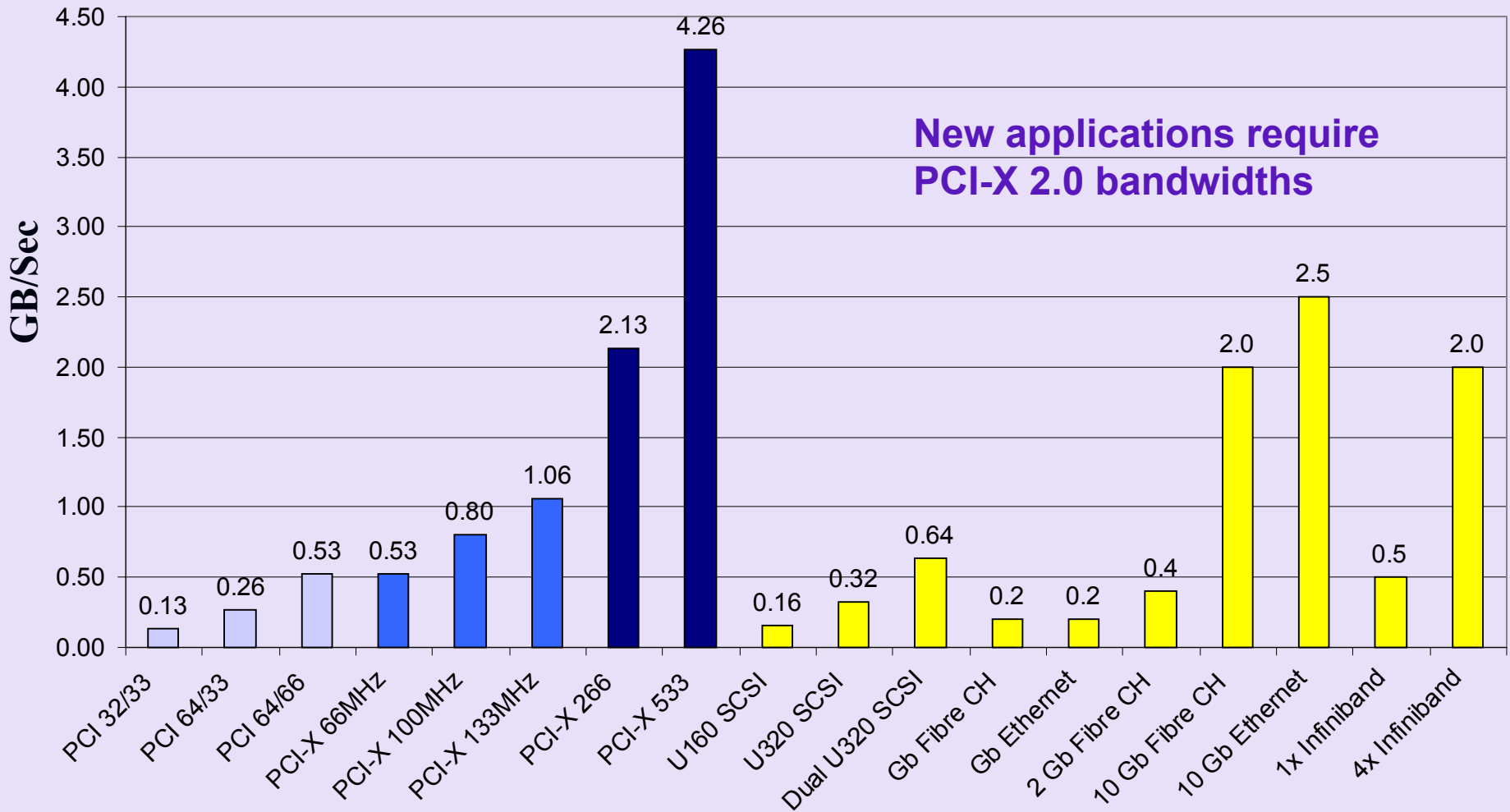
PCI-X 2.0 has 4 speed grades

Why We Need PCI-X 2.0



**Datacenters are moving to 10 Gigabit Technologies
Datacenters need PCI-X 2.0 !**

PCI-X 2.0 Bandwidth Span vs. Target Applications



PCI-X 266 and PCI-X 533 have more than enough bandwidth to support all applications.

Why PCI-X 2.0



- ✓ **Extends and improves upon the incumbent standards**
- ✓ **Evolutionary approach is easier than redesign**
- ✓ **Easy transition / simple migration**
- ✓ **Investment protection leveraging industry experience**
- ✓ **Allows cards & software reuse**
- ✓ **Engineering knowledge and design tools are already familiar**
- ✓ **Administration skills and knowledge of IT professionals is already in place.**

PCI-X 2.0 Features

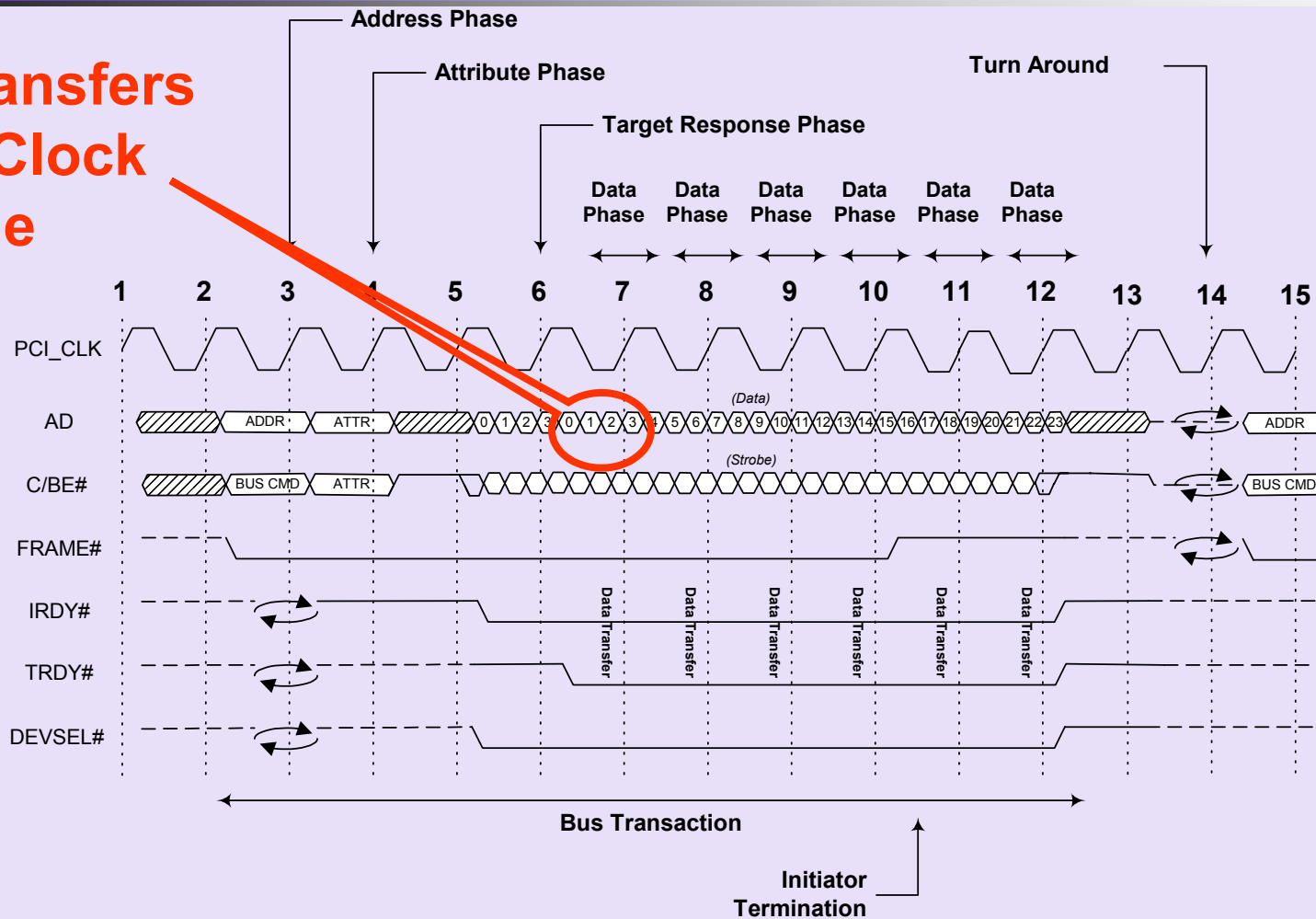


- **Same architecture**
- **Same base protocols, plus extensions**
- **Nearly identical set of signals, some with augmented functionality.**
- **Nearly identical Bus Functional Model (BFM)**
- **Software Transparent**
- **No device driver modifications**
- **Similar board level routing requirements**
- **Same connector**

PCI-X 533 Burst Write Timings



**4 Transfers
per Clock
Cycle**

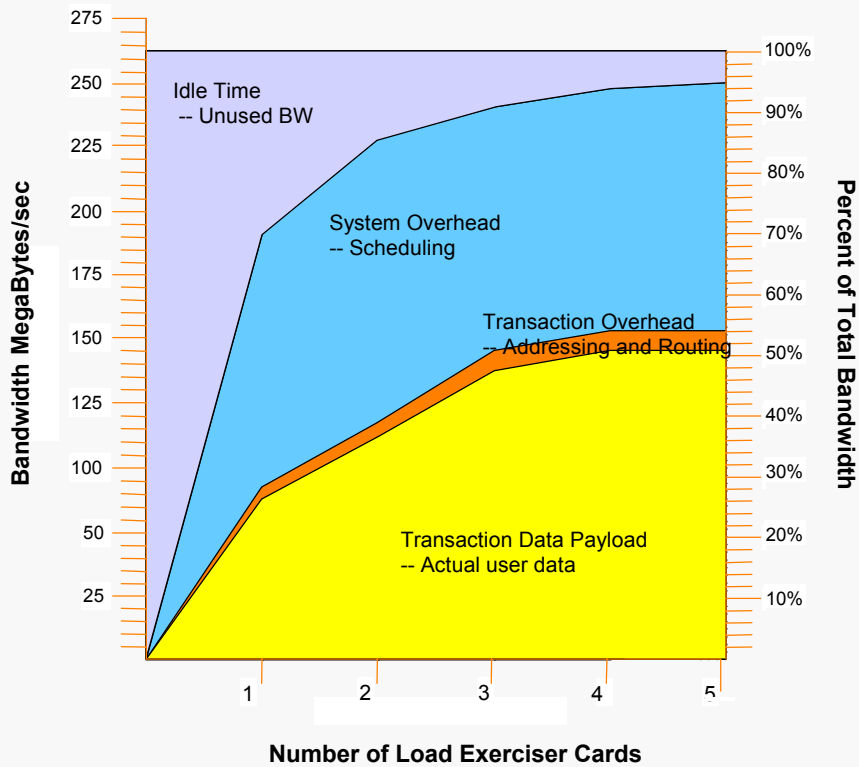


PCI-X 533 achieves high data rates by transferring 4 QWORDS of data per clock cycle.

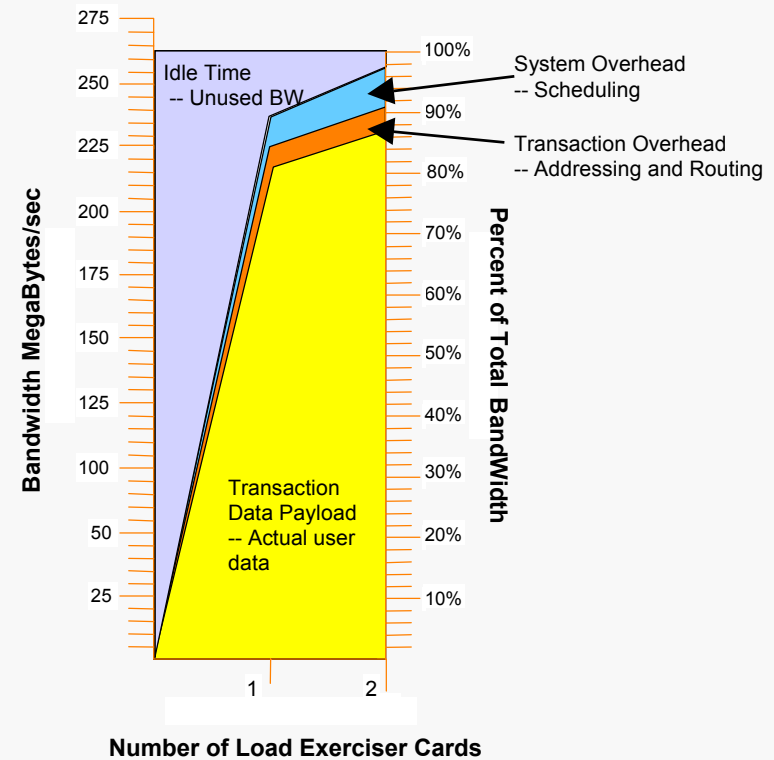
PCI-X has a More Efficient Protocol



Bandwidth Usage with Conventional PCI Protocols



Bandwidth Usage with PCI-X Protocols, included in PCI-X 2.0



The PCI-X protocol is more efficient than traditional PCI.

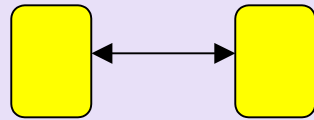
PCI-X 266 and 533 are Software Compatible with PCI



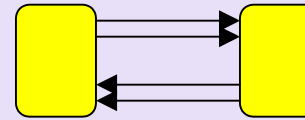
- **No OS or driver change required**
 - ✓ New configuration registers default to functional values
 - ✓ Optional performance tuning registers
 - ✓ Other configuration registers unchanged
 - ✓ No device programming model changes required
- **Optional improved error handling**
 - ✓ Enables smart device and new driver to recover from PERR# event



PCI-X 2.0 I/O Strategy



One bit of data in
PCI and PCI-X technologies:
1 single bi-directional wire.



One bit of data in serial
technologies: 4 wires --
2 for transmit,
2 for receive

PCI-X uses one wire connection for each bit of data. As a result it can operate at slower clock frequencies to transmit the same amount of data.

PCI-X 2.0 Offers Improved RAS Features



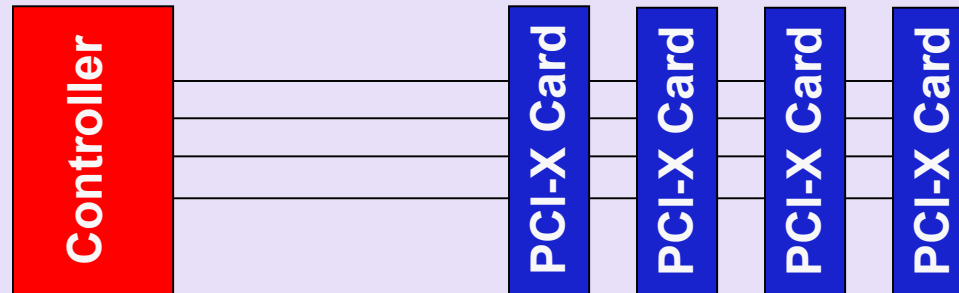
- **Parity Protection**
 - ✓ Provides full compatibility with PCI-X 1.0
- **ECC Protection**
 - ✓ Covers both header and payload.
 - ✓ Provides automatic single bit error recovery.
 - ✓ Add no additional latency over parity.
 - ✓ Replaces parity when operating with ECC enabled.
 - ✓ Optional support for parity to have compatibility with previous generations of PCI-X.

PCI-X 2.0 ECC Support



- **Supports multi-bit error detection and single bit correction on all phases**
- **Supports nibble detect and phase error detect**
- **Protects header and payload**
- **Correctable errors corrected and logged. Uncorrectable errors logged and treated like parity error in previous generations of PCI-X.**

Pin Efficient PCI-X Bus



PCI-X bus technology supports up to 4 loads with just one controller.

Multi-drop capabilities of PCI-X, provide maximum connectivity per controller pin.

- **One load – 128 pins per connection.***
- **Two loads – 64 pins per connection.***
- **Four loads – 32 pins per connection!!!***

** 32-bit bus, 66 MHz*

PCI-X 2.0 Leverages PCI-X 1.0

Simplifies Transition to PCI-X 2.0



- **Proven Infrastructure**
 - ✓ Huge Installed base of servers
 - ✓ 100's of Server Cards
 - ✓ 10's of Millions of lines of Software
 - ✓ OEM know how – relatively simple migration for systems
- **Utilizes Man Centuries of Development in PCI-X 1.0**
- **Provides Enterprise Server Protection for Next 10 Years**
- **State machine is nearly identical to the PCI-X 1.0 state machine**

PCI-X 2.0 Cost Model



- **The PCI-X 266 and PCI-X 533 cost model is the same as PCI-X 133.**
 - ✓ **Same connector**
 - ✓ **Similar protocols**
 - ✓ **Same signal functionality**
 - ✓ **Similar silicon requirements**
 - ✓ **Similar layouts**
 - ✓ **Same form factor**

1.5V I/Os for PCI-X 266 and 533



- **PCI-X 266 and 533 use new 1.5V I/Os**
 - ✓ Faster signaling rates
 - ✓ Improved noise immunity
 - ✓ New interface low-power state to manage interface power.
- **I/O Buffers also operate at 3.3V to support backward compatibility to PCI and PCI-X 133.**



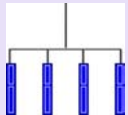
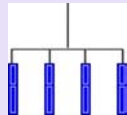
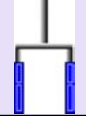
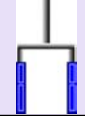
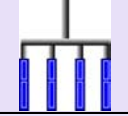
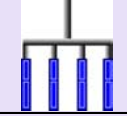
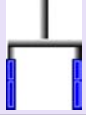
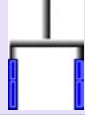






- **PCI-X 266 and PCI-X 533 add Strobes**
 - ✓ **Source-synchronous strobes improve clock timings, to enable faster data rates.**
 - ✓ **Source-synchronous strobes use sub-phases.**
 - ✓ **Strobe signals are multiplexed over existing pins.**
 - ✓ **Source-synchronous strobes simplify design by eliminating flight time issues.**

Message ID Support



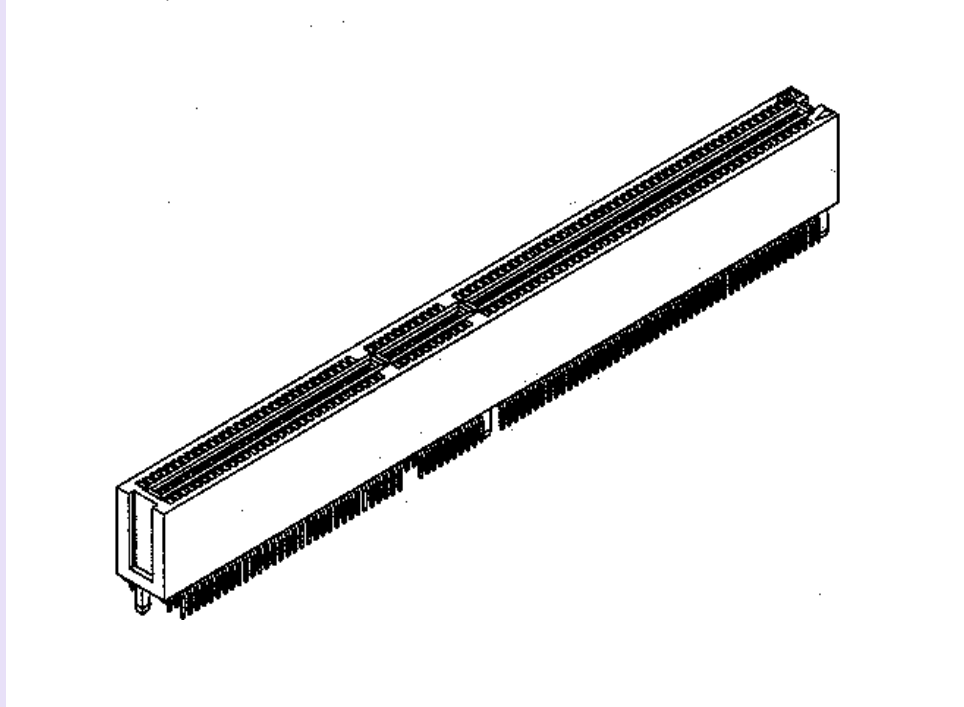
- **PCI-X 2.0 adds support for message-based transactions**
 - ✓ **All for new capabilities without adding extra signal lines.**
 - ✓ **Devices can use messages for in-band notification of events, for peer-to-peer communication, and for streaming media applications.**
 - ✓ **Implementers can define their own unique messages from the reserved codes provided in the specification to further differentiate and add value to their products.**

PCI Modes and Speeds

Mode	V _{I/O}	64-Bit		32-Bit		16-Bit
		Slots	MB	Slots	MB	
PCI 33	5V/3.3V		266		133	N/A
PCI 66*	3.3V		533		266	N/A
PCI-X 66	3.3V		533		266	N/A
PCI-X 133 (operating at 100 MHz)	3.3V		800		400	N/A
PCI-X 133	3.3V		1066		533	N/A
PCI-X 266	1.5V		2133		1066	533
PCI-X 533	1.5V		4266		2133	1066

All speed grades of PCI and PCI-X can be used to support point-to-point applications. The slower speed grades can be used to support multi-drop buses as well. Usage is dependent upon the needs of the application.

PCI-X 2.0 Connector



- PCI-X 2.0 uses the existing PCI connector.
- The same 184-pin connector that is used for PCI-X 1.0 and traditional PCI also supports PCI-X 266 and PCI-X 533.

New PCI-X 2.0 Signals



- **ECC Support**
 - ✓ 8 New signals to support ECC functionality
- **Source Synchronous Strobes**
 - ✓ 4 New strobes and complements are used
- **No new pins are needed on the connector**
 - ✓ New signals are supported by using reserved pins and by multiplexing functionality.

PCI-X 2.0 Supports Peer-to-Peer Transactions



- **Payload data is moved once across the PCI hierarchy, directly from one device to another**
 - ✓ **Improves system performance**
 - ✓ **Reduces overall system latency**
 - ✓ **Increases bandwidth utilization efficiency**



- **The PCI-X 2.0 specification introduces new 16-bit versions**
- **Ideal for low-pin-count applications that need bandwidth**
- **Builds on existing PCI infrastructure**
- **Potential applications**
 - **Embedded applications**
 - **Blade architectures**

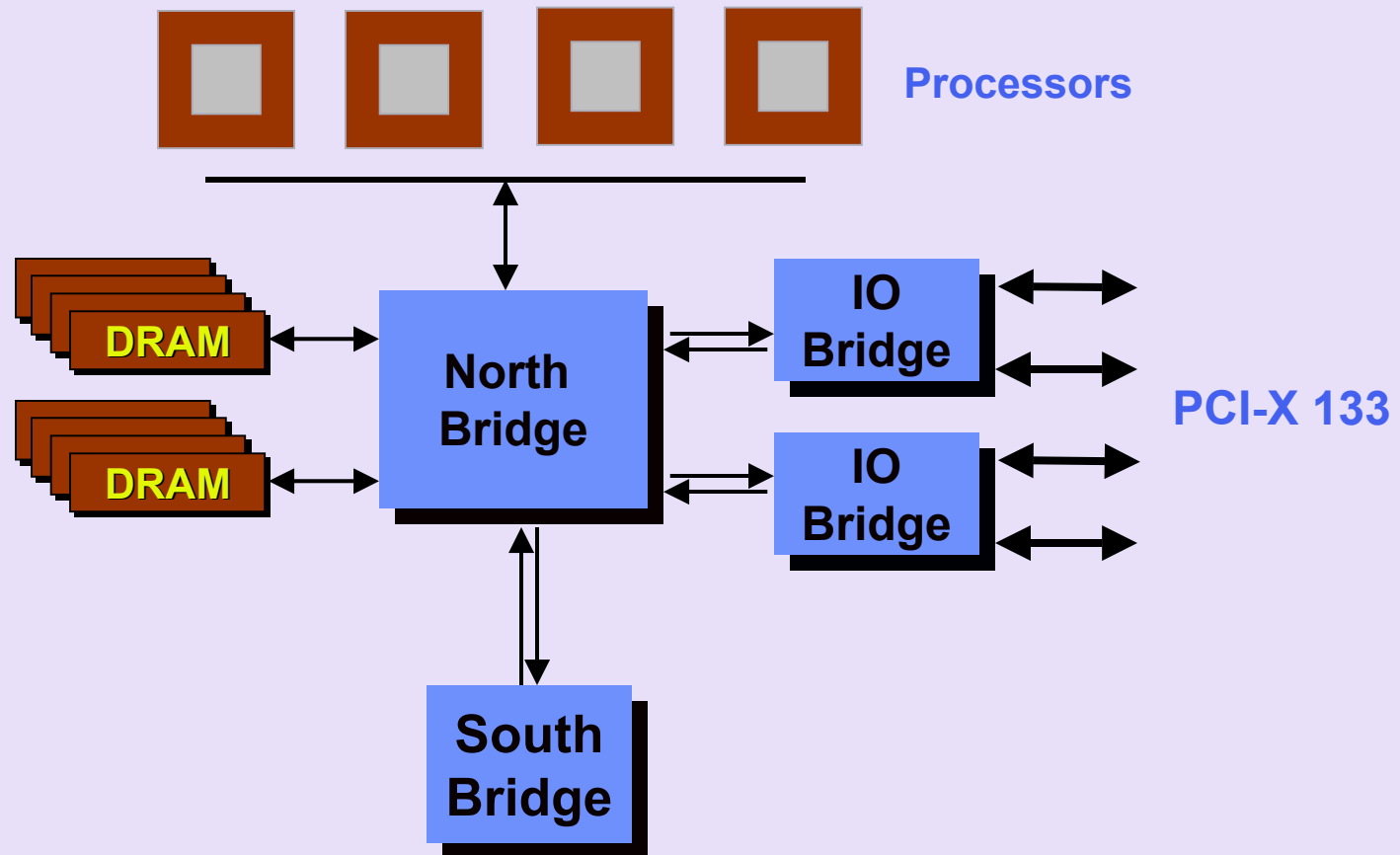
Design Elements in Place

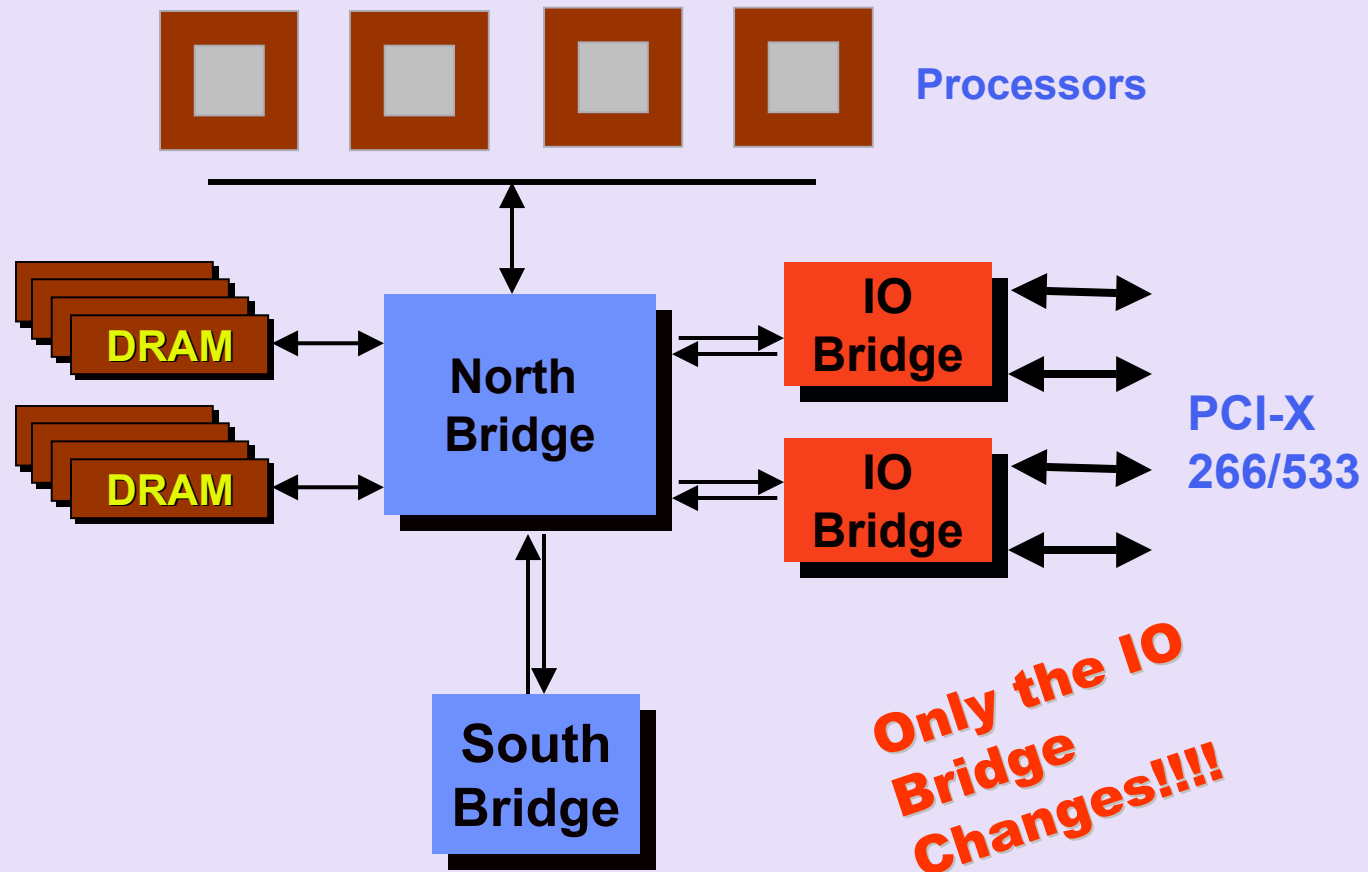


- **Nearly identical bus functional model (BFM)**
- **Software transparent**
- **No device driver modifications**
- **Minor board level routing changes**
- **Engineers already understand the technology**

PCI-X 2.0 System Design Examples

PCI-X 133 Server Platform

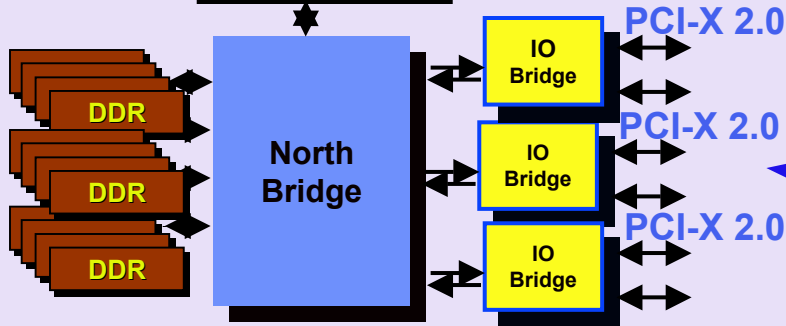




PCI-X 2.0: Top-to-Bottom

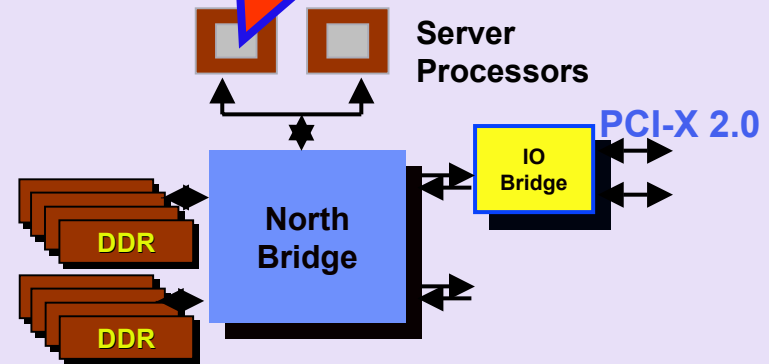
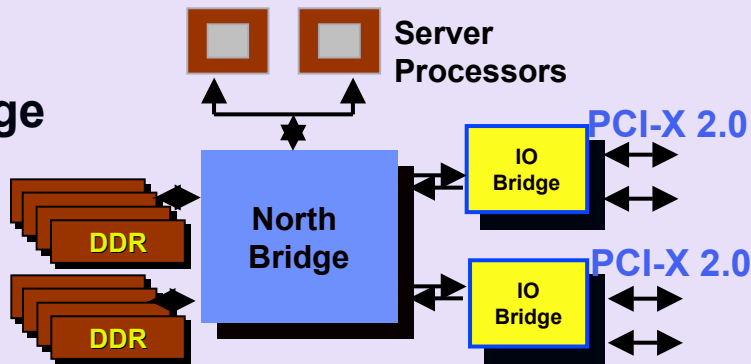


Enterprise 4-8 Way

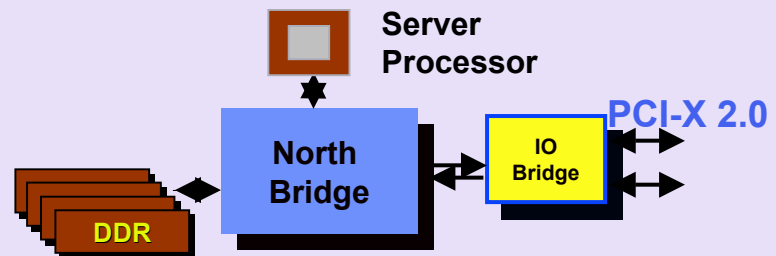
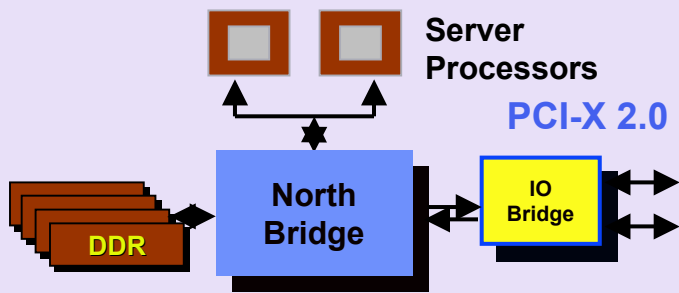


One Bridge Design Drops into All Segments!

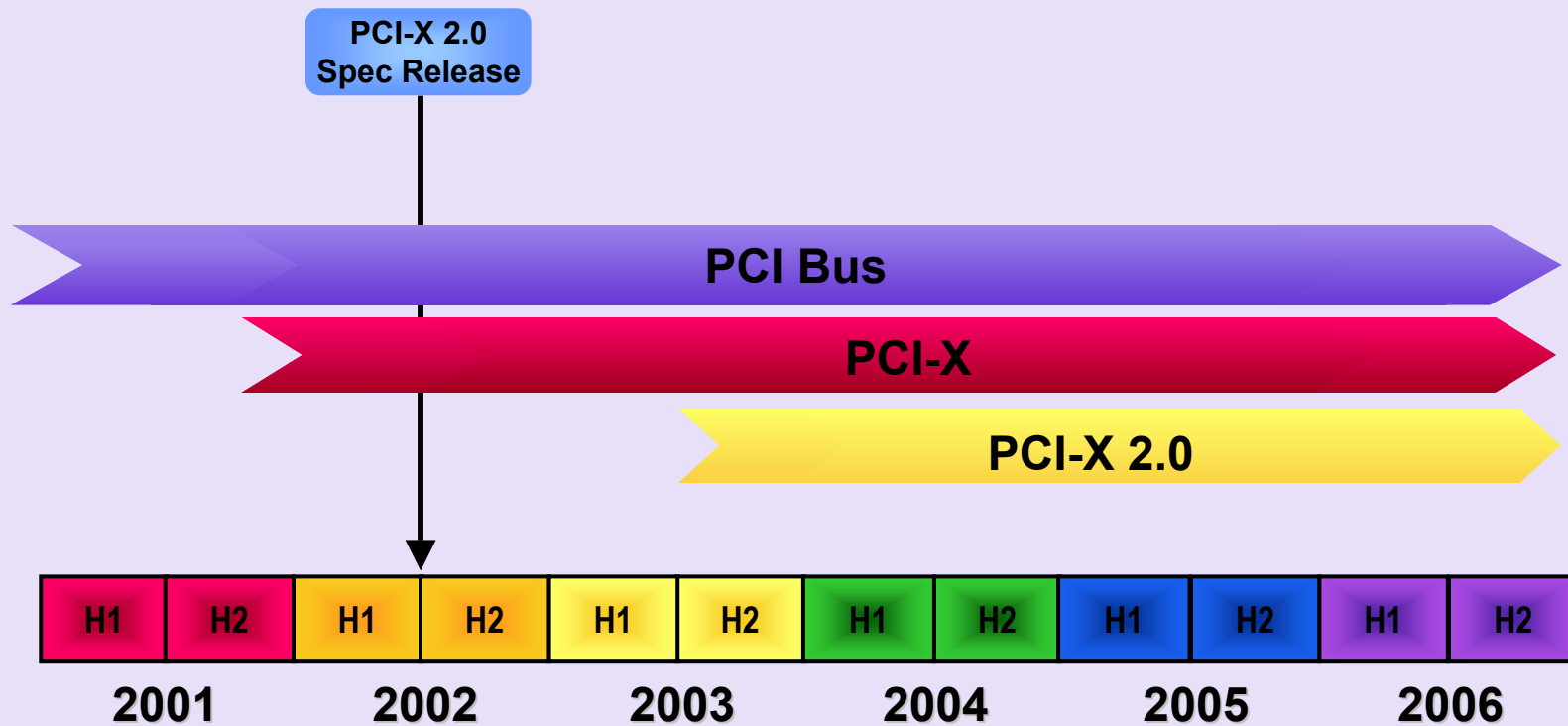
Mid-Range 2 Way



Low-end 1&2 Way



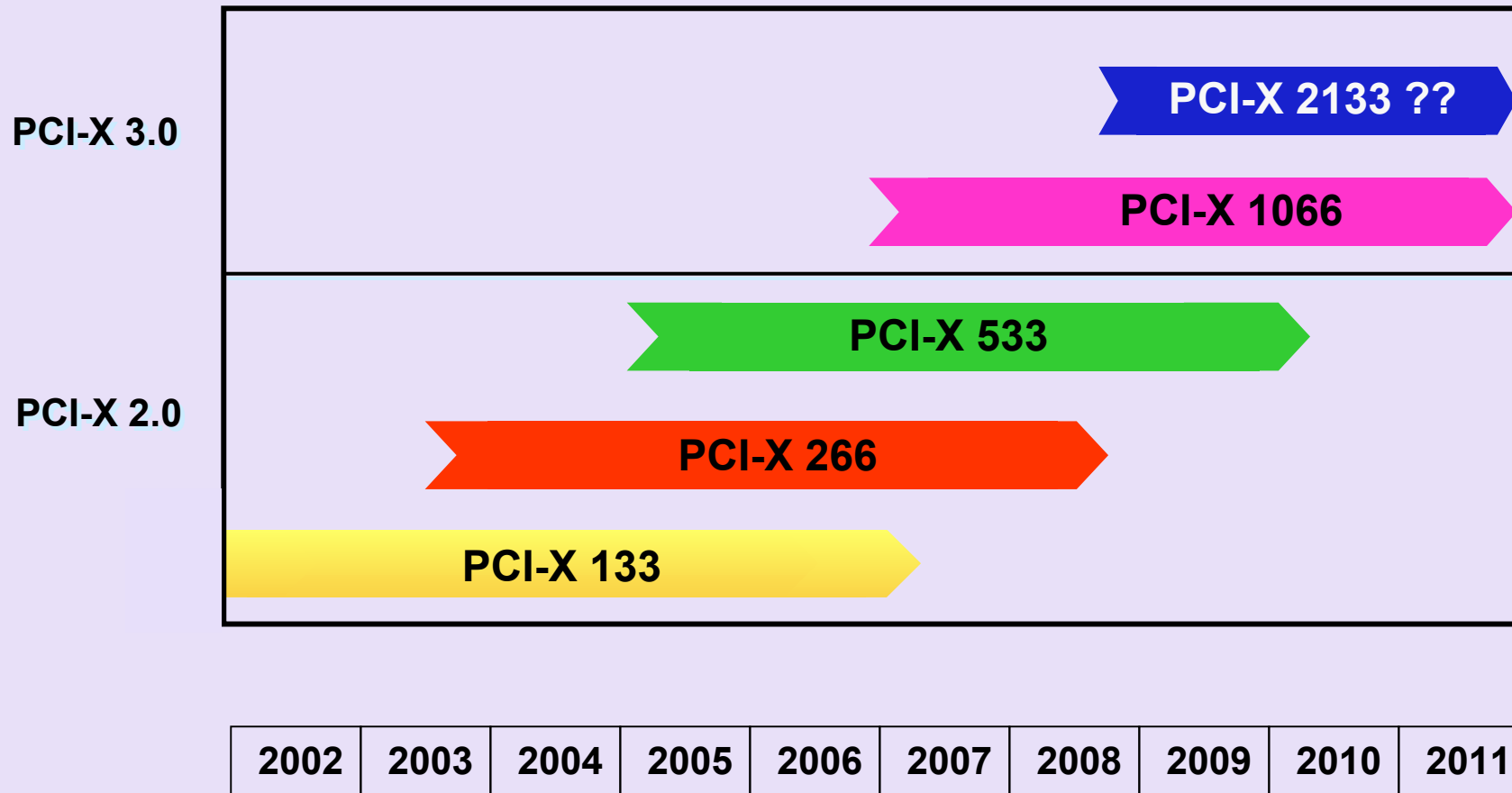
Productization Timeline



The Future of PCI-X



PCI-X Roadmap





- **The PCI-X Workgroup has begun developing PCI-X 1066.**
 - ✓ **Will double PCI-X 533 bandwidths**
 - ✓ **Will maintain backward compatibility**
 - ✓ **May include new hardware extensions – depending on PCI-SIG membership feedback.**
 - ✓ **May include new software extensions – depending on PCI-SIG membership feedback.**
 - ✓ **No change to current connector anticipated.**
- **Investigations of PCI-X 2133 are also underway.**

PCI-X 1066 Possible Hardware Extensions



- **Isochronous/Bandwidth Reservations**
- **Simplification**
 - ✓ Remove conventional PCI support >2006
 - ✓ Strictly ordered interconnect simplifies switch designs
- **Automatic Power Management—Seamless power management...No software needed**
- **Data Compression—Increases bandwidth with no change in wire speeds**
- **RAS enhancements**
 - ✓ Automatic Fail-over—Auto detection mechanism for failover
 - ✓ Redundant Paths—Routing tables for fast paths through the hierarchy
 - ✓ Performance Monitors
 - Real-time status information on interconnect
 - BW utilization by link, by card, by function, etc
 - ✓ Point-to-Point Bridges/Switch Exception Recovery — device driver/software interfaces for exception handling/recovery
- **Modular Form factors for external access.**



- **I/O Controller Engines**
 - ✓ Host DMA engines to increase performance by offloading work from the CPU's
 - ✓ Concurrent non-blocking Interfaces
 - Requires no operating system changes
- **Device ID Messaging – Peer-to-Peer**
 - ✓ Specify PCI-SIG usage model
- **Isochronous/Bandwidth Reservations**
 - ✓ Finer control of bandwidth via software linkage

PCI-X 2.0 Summary



- **100% Backward Compatible**
 - ✓ Spans all PCI, PCI-X, and PCI-X 2.0 Cards
- **One universal connector Spans 0.1 GB/s to 4.3 GB/s (32x Span!)**
- **Full RAS features for higher reliability**
- **Enough Bandwidth to Support All Applications**
- **Interoperable with all speed generations of PCI and PCI-X**
- **Leveraged Development from PCI and PCI-X base**
- **The PCI-X standard will continue to improve to meet demands of applications.**